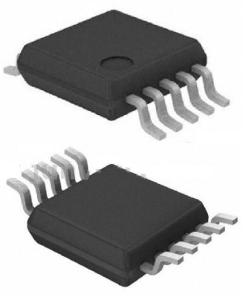
16-bit ADC with Input Multiplexer and Onboard Reference

PRODUCT DESCRIPTION

The MS1112 is a high-precision, continuously self-calibrating ADC with two differential or three single-ended input channels, up to 16 bits resolution. The on-board reference provides a differential input range of ±2.048V. The MS1112 uses an I^2C compatible interface and has two address pins, allowing users to select from eight I^2C slave addresses. The power supply range is from 2.7V to 5.5V.

The MS1112 can perform conversions at rates of 15, 30, 60 or 240 samples per second (SPS). It integrates a programmable gain amplifier(PGA), which can provide the gain up to 8, thus small signal could also be measured in ensured resolution condition. In single-conversion mode, the MS1112 automatically powers down after a conversion, greatly reducing power consumption during idle period.

The MS1112 is designed for applications requiring high-resolution measurement, where space and power consumption are major considerations.



MSOP10

FEATURES

- Data Acquisition System for Small Outline Package
- Two Differential, Three Single-ended Input Channels
- I^2C Interface, Eight Programmable Addresses
- On-board Reference : 2.048V±0.5%;
- Temperature Drift : 10ppm/°C
- On-board PGA : One to Eight
- On-board OSC
- 16 Bits No-missing Resolution
- INL (Integral Nonlinearity) : 0.01%
- Continuous Self-calibration
- Single Conversion Function
- Programmable Output Rate : 15SPS to 240SPS
- Operating Voltage : 2.7V to 5.5V
- Low Power Dissipation : 290uA

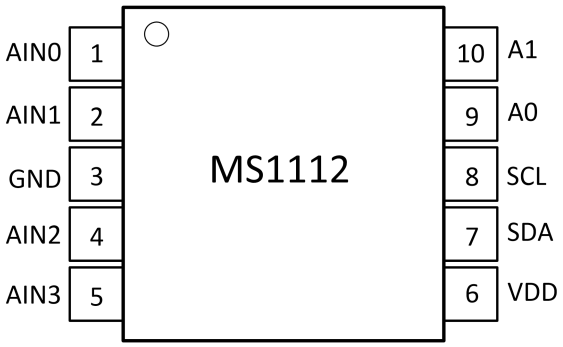
APPLICATIONS

- Portable Instrumentation
- Industrial Control
- Smart Transmitters
- Factory Automation
- Temperature Measurement

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1112	MSOP10	MS1112

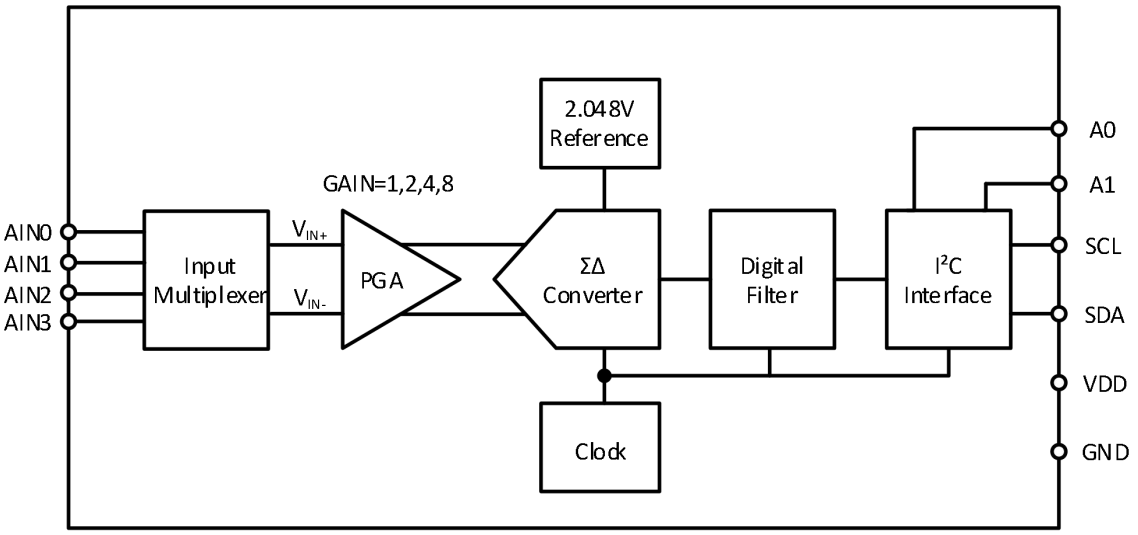
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Name	Type	Description
1	AIN0	I	Differential Input Channel 1, Positive Input/Single-ended Positive Input 1
2	AIN1	I	Differential Input Channel 1, Negative Input/Single-ended Positive Input 2
3	GND	--	Ground
4	AIN2	I	Differential Input Channel 2, Positive Input/Single-ended Positive Input 3
5	AIN3	I	Differential Input Channel 2, Negative Input/Single-ended Common Input
6	VDD	--	Power Supply
7	SDA	I/O	Serial Data Transmitting and Receiving Terminal
8	SCL	I/O	Serial Clock Input, Clock Output Terminal
9	A0	I	I^2C Salve Address Selection 1
10	A1	I	I^2C Salve Address Selection 2

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VDD	-0.3 ~ 6	V
Input Current	IIN	100mA, Momentary	mA
Input Current	IIN	10mA, Continuous	mA
Analog Input (A0,A1 to GND)	VIN	-0.3 ~ VDD+0.3	V
SDA, SCL Voltage to GND	V	-0.5 ~ 6	V
Maximum Junction Temperature	T	150	°C
Operating Temperature	T_A	-40 ~ 125	°C
Storage Temperature	Tstg	-60 ~ 150	°C
Lead Temperature(10s)	T	260	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD=5V, T_A= -40°C to 85°C.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Full-scale Input Voltage	(V_{IN+})-(V_{IN-})		±2.048/PGA		V
Analog Input Voltage	V_{IN+} to GND, V_{IN-} to GND	GND-0.2		VDD+0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-mode Input Impedance	PGA=1		3.5		MΩ
	PGA=2		3.5		MΩ
	PGA=4		1.8		MΩ
	PGA=8		0.9		MΩ
System Performance					
Resolution and No missing Codes	DR=00	12		12	Bits
	DR=01	14		14	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Output Rate	DR=00	180	240	308	SPS
	DR=01	45	60	77	SPS
	DR=10	22	30	39	SPS
	DR=11	11	15	20	SPS
Integral Nonlinearity	DR=11, PGA=1, End Point [1]		±0.004	±0.010	% of FSR [2]
Offset Error	PGA=1		8	15	mV
	PGA=2		8	15	mV
	PGA=4		8	15	mV
	PGA=8		8	15	mV
Offset Drift	PGA=1		1.2		uV/°C
	PGA=2		0.6		uV/°C
	PGA=4		0.3		uV/°C
	PGA=8		0.3		uV/°C
Offset vs VDD	PGA=1		800		uV/V
	PGA=2		400		uV/V
	PGA=4		200		uV/V
	PGA=8		150		uV/V

Parameter	Condition	Min	Typ	Max	Unit
System Performance					
Gain Error			0.05	0.4	%
PGA Gain Match Error [3]	Any two gains match		0.02	0.1	%
Gain Error Drift			10		ppm/°C
Gain vs VDD			80		ppm/V
Common-mode Rejection Ratio	DC Input, PGA=8	95	105		dB
	DC Input, PGA=1		100		dB
Digital input/Output					
Input High Level		0.7×VDD		6	V
Input Low Level		GND-0.5		0.3×VDD	V
Output Low Level	I_{OL}=3mA	GND		0.4	V
Input High Peak Current				10	uA
Input Low Peak Current		-10			uA
Power Supply					
Operating Voltage	VDD	2.7		5.5	V
Power Supply Current	Power down		0.05	2	uA
	Operation		290	350	uA
Power Dissipation	VDD=5.0V		1.45	1.75	mW
	VDD=3.0V		0.87		mW

Note：

1. 99% of full-scale.
2. FSR = full-scale range = 2 × 2.048V/PGA = 4.096V/PGA.
3. Includes all errors from PGA and reference.

FUNCTION DESCRIPTION

The MS1112 is a 16-bit, self-calibration, delta-sigma A/D converter. It ha easy design and configuration, so users can easily achieve accurate measurement.

The MS1112 consists of a delta-sigma A/D converter with adjustable gain, a 2.048V reference, a clock oscillator, a digital filter and an I^2C interface. Each of these blocks are described in detail as follows.

Analog-to-Digital Converter

The A/D converter core consists of a differential switched-capacitor delta-sigma modulator and a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs and compares it with reference voltage, which is 2.048V in the MS1112. The digital filter receives high-speed bit stream from the modulator and outputs a code, which is a number proportional to the input voltage.

Input Multiplexer

The MS1112 has a input multiplexer, which provides two differential and three single-ended input channels. The two bits of configuration register control input multiplexer setting.

Voltage Reference

The MS1112 contains an on-board 2.048V voltage reference. This reference is usually used as the ADC voltage reference, and an external reference cannot be connected. The MS1112 can only use internal voltage reference, which cannot be measured directly and used by external circuitry. The on-board reference specifications are part of the overall gain and temperature drift specifications of the MS1112. The converter drift and gain error specifications reflect the performance of the on-board reference and the A/D converter core. There are no separate specifications for the on-board reference itself.

Output Code Calculation

The output code is a scaled value that is proportional, except for clipping, to the voltage difference between the two analog inputs. The output code is confined to a finite numbers range, which depends on the number of bits needed to represent the code. The number of bits needed to represent the output code for the MS1112 depends on the data rate, as shown in Table 1.

Table 1. Minimum and Maximum Code

Data Rate	Number Of Bits	Minimum Code	Maximum Code
15SPS	16	-32768	32767
30SPS	15	-16384	16383
60SPS	14	-8192	8191
240SPS	12	-2048	2047

For minimum output code of minimum code, gain setting of the PGA, and positive and negative input voltages of VIN+ and VIN−, the output code is given by the expression:

$$\text{Output Code} = -1\times\text{Minimum Code}\times\text{PGA}\times\frac{(V_{IN+})-(V_{IN-})}{2.048V}$$

In the previous expression, it is important to note that the negative minimum output code is used. The MS1112 output code format, is binary two's complement, so the absolute values of the minimum and maximum are not the same. The maximum n-bit code is $2^{n-1}-1$, while the minimum n-bit code is $-1\times2^{n-1}$.

For example, the ideal expression for output code with data rate of 30SPS and PGA=2 is:

$$\text{Output Code} = 16384 \times 2 \times \frac{(V_{IN+})-(V_{IN-})}{2.048V}$$

All the MS1112 output codes are right-justified and sign-extended. This feature makes it possible to perform averaging on the higher data rate codes using only a 16-bit accumulator. Table 2 shows the output codes for various input levels.

Table 2. Output Codes for Different Input Signals

Data Rate	Differential Input Signal				
	-2.048V[1]	-1LSB	ZERO (Ideal)	+1LSB	+2.048V
15SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
30SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
60SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
240SPS	$F000_H$	$FFFF_H$	0000_H	0001_H	$0FFF_H$

Note 1: Differential input only; do not drive the MS1112 input voltage below −200mV.

Self-Calibration

As previous expressions given, the MS1112 output code do not include the gain and offset errors of the modulator. To compensate for these, the MS1112 integrates self-calibration circuitry.

The self-calibration system operates continuously and doesn't require user intervention. Self-calibration system can't be adjusted, doesn't need adjustment and cannot be off. The offset and gain error figures shown in the Electrical Characteristics include the calibration effects.

Clock Oscillator

The MS1112 features an on-board clock oscillator, which drives the operation of the modulator and digital filter. The Characteristics Curves show variations in data rate over power supply and temperature. It is not possible that the MS1112 operates with an external system clock.

Input Impedance

The MS1112 uses switched-capacitor input stage. For external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor value and switching frequency. The switching frequency is the same as the modulator frequency. The capacitor value depend on the PGA setting. The switching clock is generated by on-board clock oscillator, so its frequency (normally 275kHz) is dependent on power supply and temperature.

The common-mode and differential input impedance is different. For PGA gain, the differential input impedance is 2.8MΩ/PGA typically. The common-mode impedance also depends on the PGA setting.

The typical value of input impedance cannot be neglected normally. Unless the input source has low impedance, the MS1112 input impedance may affect the measurement resolution. For source with high output impedance, buffering should be necessary. However, that active buffer may introduce noise offset and gain error. All of these factors should be considered in high-resolution applications. Because the clock oscillator frequency drifts slightly over temperature, the input impedance will also generate drift. For many applications, input impedance drift can be neglected, and the above typical input impedance can be used .

Aliasing

If the MS1112 input signal frequency exceeds half the data rate, aliasing will occur. To prevent aliasing, the input signal bandwidth must be limited, and some signals itself have bandwidth limit. For example, the output of thermocouple with limited change rate, still includes noise and interference. And these interference factors can be aliased into sampling band like other signals. The MS1112 digital filter can attenuates high-frequency noise to some extent, but Sinc1 frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed. In such instances, a simple RC filter will be enough.

When designing an input filter circuit, remember to take into account the interaction between the filter network and the input impedance of the MS1112.

Operating Modes

The MS1112 operates in one of two modes: continuous conversion or single conversion.

In continuous conversion mode, once a conversion has been completed, the MS1112 places the result in the output register and immediately begins another conversion.

In single conversion mode, the MS1112 waits until the ST/DRDY bit of the conversion register is set as 1. When this happens, the MS1112 powers up and performs in single conversion mode. After the conversion finishes, the MS1112 places the result in the output register, resets the ST/DRDY bit to 0 and powers down. While a conversion is in progress, writing 1 to ST/DRDY has no effect.

When switched from continuous conversion mode to single conversion mode, the MS1112 completes the current conversion, resets the ST/DRDY bit to 0 and powers down.

Reset and Power-Up

When the MS1112 powers up, it automatically performs one reset. As part of the reset process, the MS1112 sets all of the bits in the configuration register as their default settings.

The MS1112 responds to the I^2C general call reset command. When the MS1112 receives a general call reset, it performs an internal reset, exactly as though it had just been powered up.

I^2C Interface

The MS1112 communicates through an I^2C interface. I^2C interface is a two-wire open drain output interface, which supports several devices and shares one bus with master. Devices on the I^2C bus only drive the bus low by connecting them to ground, and they can't drive the bus high. Instead, the bus is pulled high by pull-up resistors, so the bus is high when no device drives it low. This way makes two devices without conflict. If two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other as the slave. Both master and slave can read and write, but slave can only do so under the direction of the master. Some I^2C devices can act as master or slave, but the MS1112 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides clock. All data is transmitted across the I^2C bus in groups of eight bits. In order to transmit a bit on the I^2C bus, SDA line is driven to the appropriate level while SCL is low (Low on SDA indicates the bit is zero; High indicates the bit is one). Once SDA line has settled, SCL line is pulled high, then becomes low. The pulse on SCL clocks the SDA bit into the receiver's shifting register.

The I²C bus is bidirectional: SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends data to a slave, the master drives the data line. The master always drives the clock line. The MS1112 never drives SCL, because it cannot act as a master. For the MS1112, SCL is an input only.

Most of the time, the bus is idle. No communication occurs, and both lines are high. When in communication, the bus is active. Only master device can start one communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state, while the clock line is low. If when the clock line is high, the data line changes state, thus it forms either a START condition or its counterpart, a STOP condition. A START condition occurs when the clock line is high and the data line goes from high to low. A STOP condition occurs when the clock line is high and the data line goes from low to high.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on I²C bus has a unique 7-bit address to respond. The master sends an address in the address byte, together with a bit that indicates whether it reads from or writes to the slave device.

Every byte transmitted on the I²C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending one byte (eight data bits) to a slave, it stops driving SDA line and waits for the slave to respond to the byte. The slave acknowledges the byte by pulling SDA line low. Then the master sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading one byte, it pulls SDA line low to respond to the slave. It then sends a clock pulse to clock the bit (Remember that master always drives clock line).

During an acknowledge cycle, a not-acknowledge is performed by simply leaving SDA line high . If a device is not present on the bus, and if the master attempts to address it, it will not receive acknowledge signal, because there is no device on the address to pull SDA line low.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. If a START condition is issued while the bus is active, a repeated START condition is required.

A timing diagram for MS1112 I²C is shown in Figure 1. The related parameters for this diagram are given in Table 3.

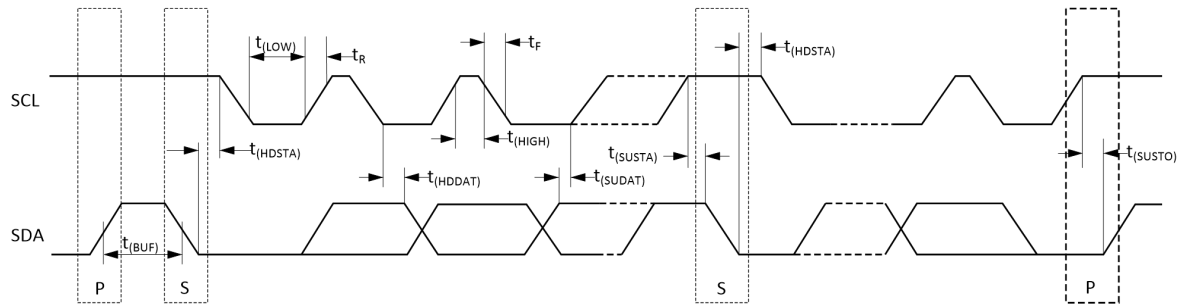


Figure 1. I²C Timing Diagram

Table 3. Related Parameters of Timing Diagram

Parameter	Fast-Speed Mode		High-Speed Mode		Unit
	Min	Max	Min	Max	
SCLK Operating Frequency $t_{(SCLK)}$		0.4		3.4	MHz
Bus START to STOP Idle Time $t_{(BUF)}$	600		160		ns
START Hold Time $t_{(HDSTA)}$	600		160		ns
Repeated START Setup Time $t_{(SUSTA)}$	600		160		ns
STOP Setup Time $t_{(SUSTO)}$	600		160		ns
Data Hold Time $t_{(HDDAT)}$	0		0		ns
Data Setup Time $t_{(SUDAT)}$	100		10		ns
SCLK Clock Low Level Period $t_{(LOW)}$	1300		160		ns
SCLK Clock High Level Period $t_{(HIGH)}$	600		60		ns
Clock/Data Fall Time t_F		300		160	ns
Clock/Data Rise Time t_R		300		160	ns

Serial Bus Address

In order to read from and write to the MS1112, the master must first address to the slave through address bit. The slave address includes seven address bits and one operation bit, which indicate read or write operation.

The MS1112 has two address pins, A0 and A1, setting I^2C address. The pin could be set as logic ground, high or NC(Float). Eight different addresses can be set through the two pins, as shown in table 4. After power-up-reset or I^2C communication, A0 and A1 pin states are sampled and should be set before interface activation.

Table 4. MS1112 Address Pins and Slave Address

A0	A1	Slave Address
0	0	1001000
0	Float	1001001
0	1	1001010
1	0	1001100
1	Float	1001101
1	1	1001110
Float	0	1001011
Float	1	1001111
Float	Float	Invalid

I²C General Call

If the eight address is 0, the MS1112 would respond to general call. The device acknowledges and respond in the second byte command. If the command is 04h, the MS1112 would latch the states of address pins of A0 和 A1 without reset. If the command is 06h, the MS1112 would latch the state of address pin and reset internal register.

I²C Data Rate

I²C bus operates in one of the three speed modes: standard mode, allowing the clock frequency up to 100kHz; fast-speed mode, allowing the clock frequency up to 400kHz; high-speed mode(Hs), allowing the clock frequency up to 3.4MHz. The MS1112 is completely compatible with these modes.

No special operation is needed to make the MS1112 in standard or fast-speed mode, while adopting high-speed mode must be activated. In order to activate high-speed mode, first send a special address byte 00001xxx after the START condition, where xxx is only appropriate to the master adopting Hs mode. The byte is called Hs master code (Note that it is different from normal address byte, and the lowest bit doesn't indicate read/write state). The MS1112 will not acknowledge the byte. The I²C specification forbids the acknowledgment of the Hs master code. When receives the master code, the MS1112 would enable high-speed mode filter, and communicates on clock frequency up to 3.4MHz. When next STOP condition, the MS1112 would switch out of Hs mode.

Registers

The MS1112 has two registers that are accessible via its I²C port. The output register contains the result of the last conversion. The configuration register allows the user to change the MS1112 operating mode and query device status.

Output Register

The 16-bit output register contains the result of the last conversion in binary two's complement format. After reset or power-up, the output register is cleared to zero, and remains zero until the first conversion is completed. The output register format is shown in Table 5.

Table 5. Output Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Register

The 8-bit configuration register can be used to control the MS1112 operating mode, data rate and PGA setting. The configuration register format is shown in Table 6. The default setting is $8C_H$.

Table 6. Configuration Register

BIT	7	6	5	4	3	2	1	0
NAME	ST/DRDY	INP1	INP0	SC	DR1	DR0	PGA1	PGA0
DEFAULT	1	0	0	0	1	1	0	0

Bit 7: ST/DRDY

The meaning of the ST/DRDY bit depends on whether it is being written to or read from.

In single conversion mode, writing 1 to the ST/DRDY bit causes starting a conversion, and writing 0 has no effect. In continuous conversion mode, the MS1112 ignores the value written to ST/DRDY.

When performing read operation, ST/DRDY indicates whether the data in the output register is new data. If ST/DRDY is 0, the data just read from the output register is new, which has not been read before. If ST/DRDY is 1, the data just read from the output register has been read before.

The MS1112 sets ST/DRDY as 0 when it writes data to the output register. It sets ST/DRDY as 1 after any of the bits in the configuration register have been read. (Note that the read value of the bit is independent of the value written to this bit.)

In continuous conversion mode, use ST/DRDY to determine when new conversion data is ready. If ST/DRDY is 1, the data in the output register has already been read, and is not new. If it is 0, the data in the output register is new, and has not yet been read.

In single conversion mode, use ST/DRDY to determine whether a conversion has completed. If ST/DRDY is 1, the output register data is old, and the conversion is still in process. if it is 0, the output register data is the result of the new conversion.

Note that the output register is returned from the MS1112 before the configuration register. The state of the ST/DRDY bit is appropriate to the data just read from the output register, rather than the data from the next read operation.

Bit 6-5 : INP

INP controls two ADC input signals of four analog inputs, as shown in table 7. Through the two bits, the MS1112 can be used to measure two differential channels, or three single-ended input channels referenced to AIN3.

Table 7. INP Bit

INP1	INP0	VIN+	VIN-
0[1]	0[1]	AIN0	AIN1
0	1	AIN2	AIN3
1	0	AIN0	AIN3
1	1	AIN1	AIN3

Note 1: Default setting

Bit 4 : SC

SC bit controls whether the MS1112 is in continuous or single conversion mode. When SC is 1, the MS1112 is in single conversion mode. When SC is 0, it is in continuous conversion mode. The default setting is 0.

Bit 3-2 : DR

Bits 3 and 2 control the MS1112 data rate, as shown in Table 8.

Table 8. DR Bit

DR1	DR0	Data Rate	Resolution
0	0	240SPS	12 Bit
0	1	60SPS	14 Bit
1	0	30SPS	15 Bit
1[1]	1[1]	15SPS	16 Bit

Note 1: Default setting

Bit 1-0 : PGA

Bits 1 and 0 control the MS1112 gain setting, as shown in Table 9.

Table 9. PGA Bit

PGA1	PGA0	Gain
0[1]	0[1]	1
0	1	2
1	0	4
1	1	8

Note 1: Default setting

Reading from the MS1112

To read the output register and the configuration register from the MS1112, first address the MS1112, then read three bytes. The first two bytes will be the output register's contents, and the third will be the configuration register's contents.

It is not required to read the configuration register byte. It is allowed to read fewer than three bytes during read operation. Reading more than three bytes from the MS1112 has no effect. All bytes following the fourth will be FF_H.

It is possible to ignore the ST/DRDY bit and read data from the MS1112 output register at any time, regardless of whether a new conversion completes. If the output register is read more than once during a conversion cycle, it will return the same data each time. New data will be returned only when the output register has been updated. A typical timing diagram of the MS1112 read operation is shown in Figure 2.

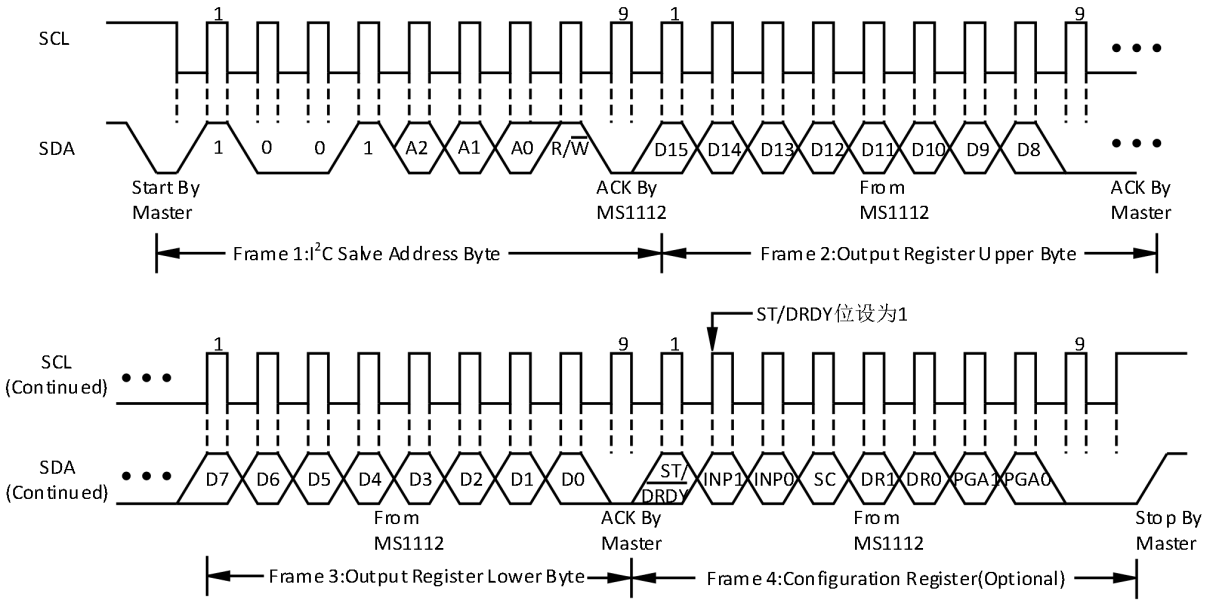


Figure 2. Timing Diagram of the MS1112 Read Operation

Writing to the MS1112

To write to the configuration register, first address the MS1112 for writing to one byte. The byte will be written to the configuration register. Note that data cannot be written to the output register.

Writing more than one byte to the MS1112 has no effect. The MS1112 will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte. A typical timing diagram of the MS1112 write operation is shown in Figure 3.

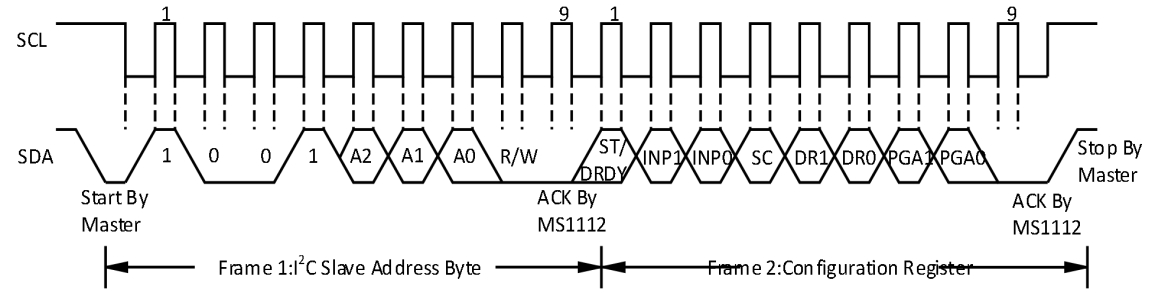
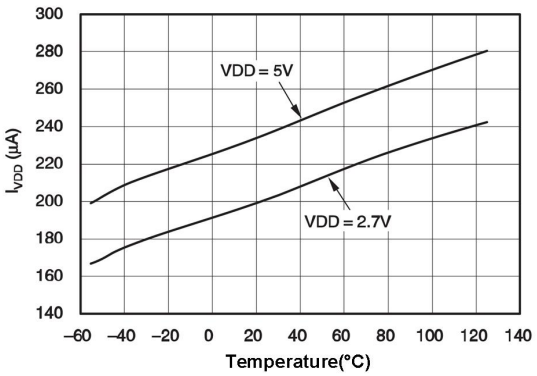


Figure 3. Timing Diagram of the MS1112 Write Operation

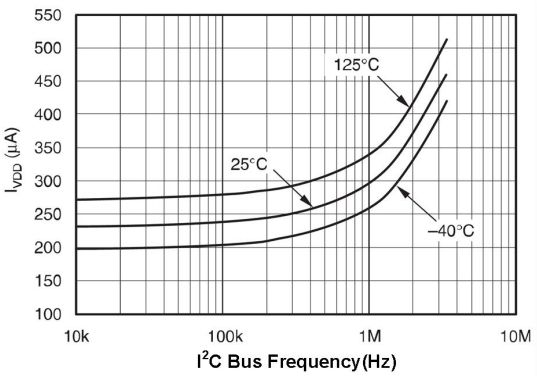
CHARACTERISTICS CURVES

Unless otherwise noted, VDD=5V, TA=25°C.

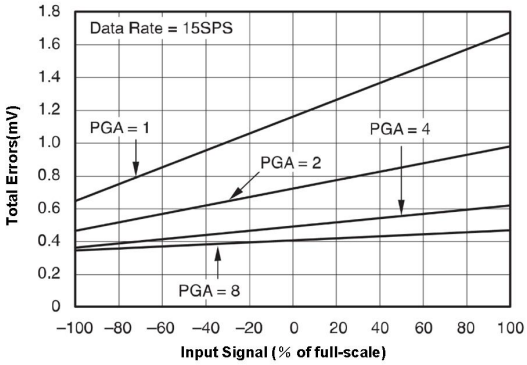
Power Supply Current VS. Temperature



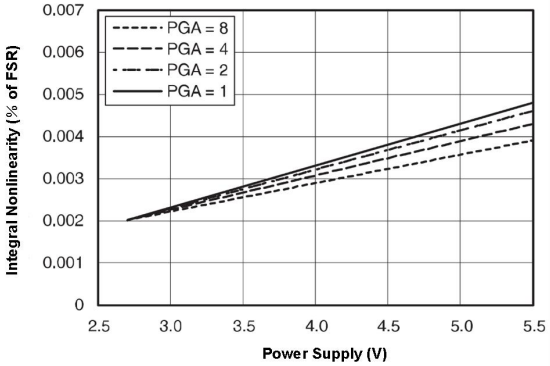
Power Supply Current VS. I²C Bus Frequency



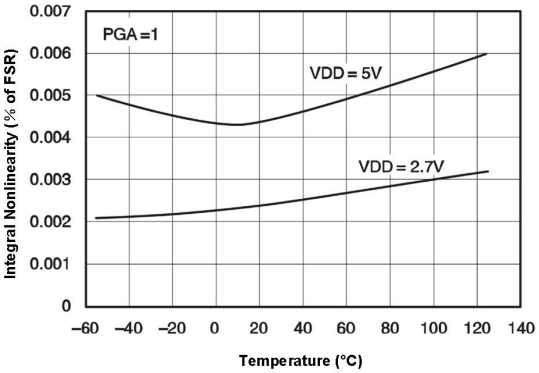
Total Errors VS. Input Signal



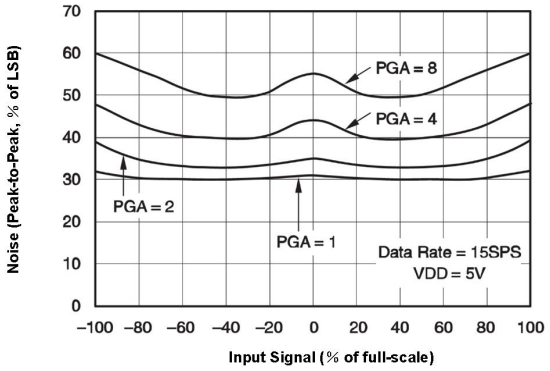
Integral Nonlinearity VS. Power Supply

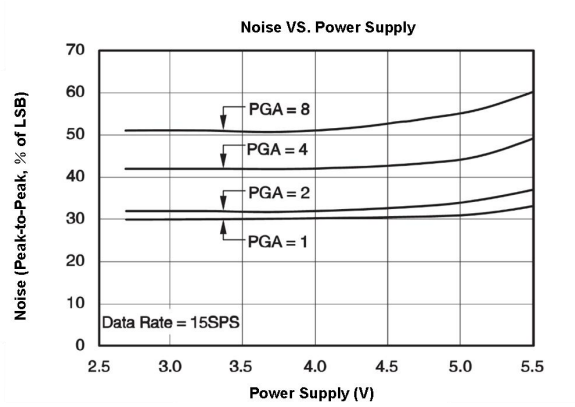


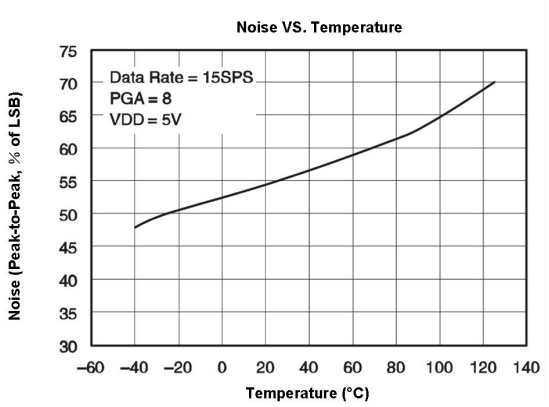
Integral Nonlinearity VS. Tempeature

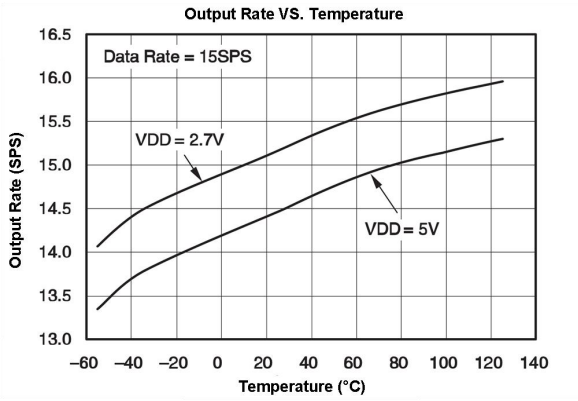


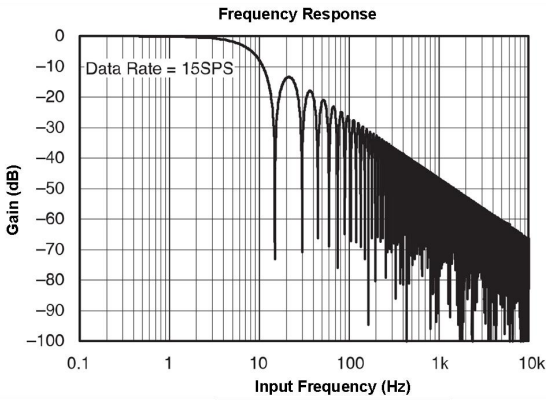
Noise VS. Input Signal




Noise VS. Power Supply
Noise (Peak-to-Peak, % of LSB)
70
60
50
40
30
20
10
0
PGA = 8
PGA = 4
PGA = 2
PGA = 1
Data Rate = 15SPS
2.5
3.0
3.5
4.0
4.5
5.0
5.5
Power Supply (V)


Noise VS. Temperature
Noise (Peak-to-Peak, % of LSB)
75
70
65
60
55
50
45
40
35
30
Data Rate = 15SPS
PGA = 8
VDD = 5V
–60
–40
–20
0
20
40
60
80
100
120
140
Temperature (°C)


Output Rate VS. Temperature
Output Rate (SPS)
16.5
16.0
15.5
15.0
14.5
14.0
13.5
13.0
Data Rate = 15SPS
VDD = 2.7V
VDD = 5V
–60
–40
–20
0
20
40
60
80
100
120
140
Temperature (°C)


Frequency Response
Gain (dB)
0
–10
–20
–30
–40
–50
–60
–70
–80
–90
–100
Data Rate = 15SPS
0.1
1
10
100
1k
10k
Input Frequency (Hz)

TYPICAL APPLICATION DIAGRAM

The following sections list MS1112 example circuits and related information in differential applications

Basic Connection

For many applications, connecting the MS1112 is extremely simple. A basic connection diagram for the MS1112 is shown in Figure 4.

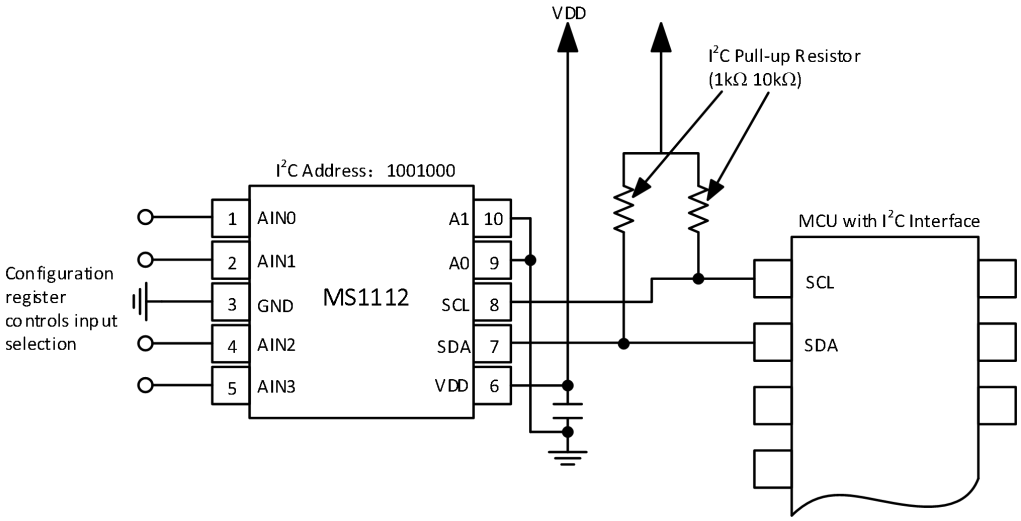


Figure 4. Typical Connection of the MS1112

The fully differential voltage input of the MS1112 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the MS1112 can read bipolar differential signals, it cannot receive negative voltages on input terminal. The user can think of the MS1112 positive input voltage as noninverting, and of the negative input as inverting.

When the MS1112 is converting, it draws current in short spikes. The 0.1μF bypass capacitor provides the momentary pulses for needed extra current from the power supply.

The MS1112 interfaces directly to I^2C controllers of standard mode, fast-speed mode, and high-speed mode. Any microcontroller's I^2C peripheral, including master-only and single-master I^2C peripherals, will work with the MS1112. The MS1112 does not perform clock-stretching (i.e.,it never pulls the clock line low), unless other devices are on the same I^2C bus.

Pull-up resistors are necessary for both the SDA and SCL lines, because I^2C bus drivers are open-drain. The value of these resistors depends on the bus operating speed and bus capacitance. Higher-value resistors consume less power dissipation, but increase the bus transition time, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power dissipation. Long bus has higher capacitance and require smaller pull-up resistors to compensate. The resistors should not be too small. If they are, the bus drivers may not be able to pull the bus low.

Connecting Multiple Devices

Connecting multiple MS1112s to the same bus is common. The MS1112 is available in eight different I^2C addresses using A1 and A0 pins. An example showing three MS1112s connected on a single bus is shown in Figure 5. Up to eight MS1112s can be connected to a single bus (using different states of A1 and A0 pins).

Note that only one set of pull-up resistors is needed per bus. The user might find that need to lower the pull-up resistance slightly to compensate for the additional bus capacitance presented by multiple devices and increase line length.

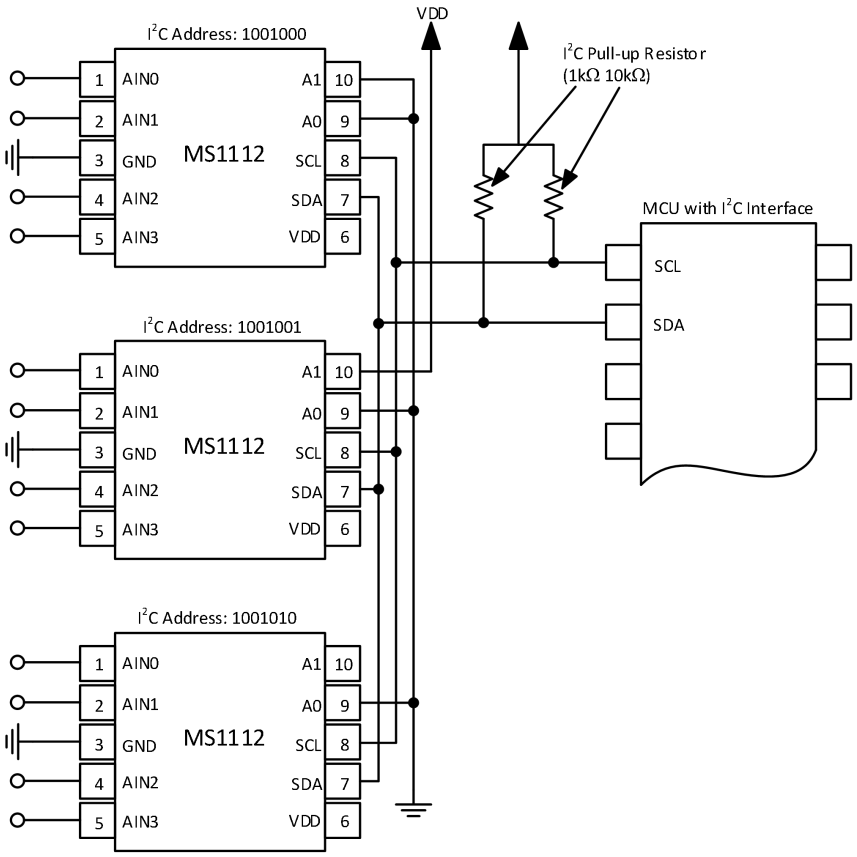


Figure 5. Connecting Multiple MS1112s

Using GPIO Ports For I²C

Most microcontrollers have programmable input/output pins that can be set as inputs or outputs by software. If an I²C controller is not available, the MS1112 can be connected to GPIO pins, and the I²C bus protocol can be simulated or generate bit-pulse by software. An example that a single MS1112 is connected to GPIO is shown in Figure 6.

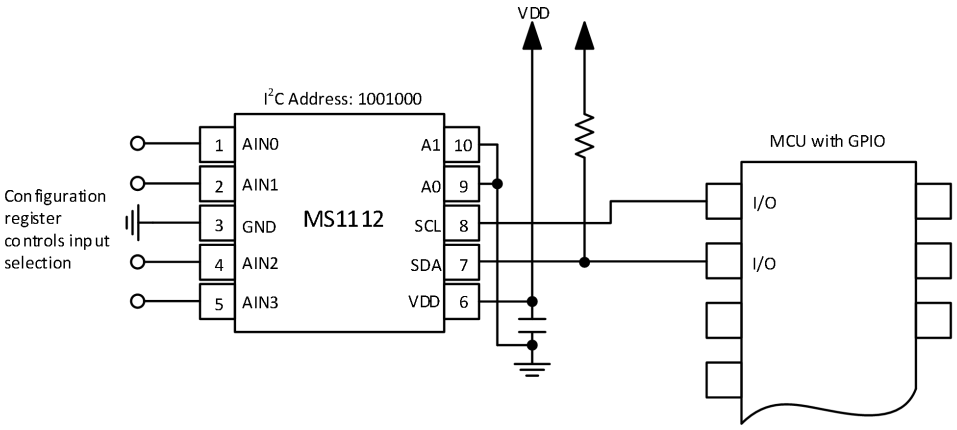


Figure 6. Using GPIO with a single MS1112

Bit-banging I²C with GPIO pins can be done by setting the GPIO line to zero and finding appropriate bus state switched between input and output modes . To drive GPIO line low, the pin is set to output zero. To drive GPIO line high, the pin is set as input terminal, and the state can be read. if another device pulls GPIO line low, zero will be read from the input register of this port.

Note that no pull-up resistor is on the SCL line. In this simple case, the resistor is not needed. The microcontroller can simply leave the line in output state, and set it to one or zero on appropriate time. It can do this because the MS1112 never drives the clock line low. This technique can also be used in multiple devices, and has the advantage of lower current consumption due to no pull-up resistor.

If there is any device on the bus that may drive clock line low, the above method should not be used. SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note that this cannot be done on the SDA line in any case, because the MS1112 drives the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pull-up circuits built in to their GPIO ports. In some cases, these can be switched on and used as external pull-up resistors. Some microcontrollers also provides weak pull-up circuits, but usually these are too weak for I²C communication. If there is any question about the matter, test the circuit before committing it to production.

Single-Ended Input

Although the MS1112 only has two differential channels, it can easily measure single-ended signals. A simple single-ended connection diagram is shown in Figure 7. The MS1112 is configured as single-ended input mode by connecting AIN3 to ground and signal to AIN0, AIN1or AIN2. According to configuration register setting, one of input signals is read out. At this time, the single-ended input signal can range from 0V to 2.048V without linearity error. Negative voltage can't be applied to this circuit, because the MS1112 can only accept positive voltage.

The MS1112 input range is relative to the reference, i.e. 2.048V bipolar differential. The single-ended circuit shown in Figure 7 only covers half the MS1112 input range, because it does not produce differential negative inputs, therefore, one bit of resolution is lost.

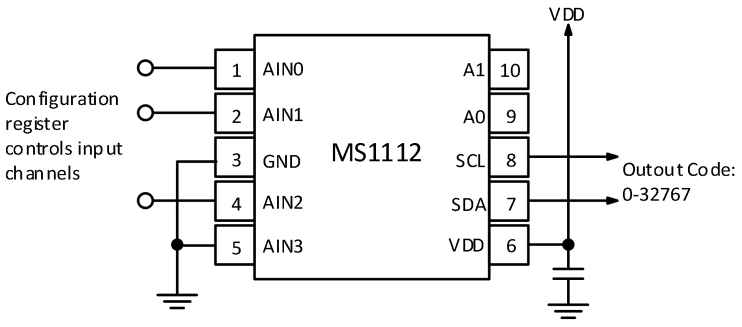


Figure 7. Single-ended Input Measurement

Low-Side Current Monitor

Figure 8 shows circuit diagram for low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is as small as possible while still giving a readable output voltage. This voltage is amplified by MS8552, and the result is read by the MS1112.

It is suggested that the MS1112 be operated at gain of 8. The gain of the MS8552 can be lowered. For gain of 8, the operational amplifier should provide maximum output voltage of no greater than 0.256V. If the shunt resistor provides maximum voltage drop of 64mV at full-scale current, the full-scale input voltage of the MS1112 is 0.2V.

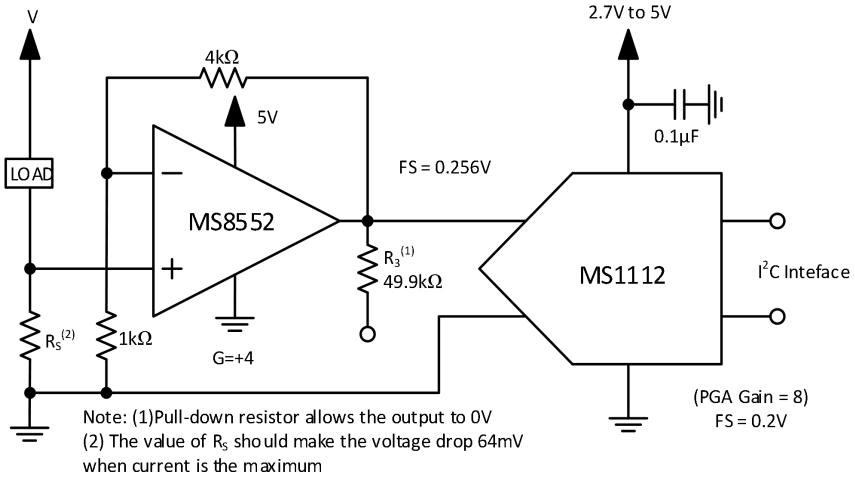
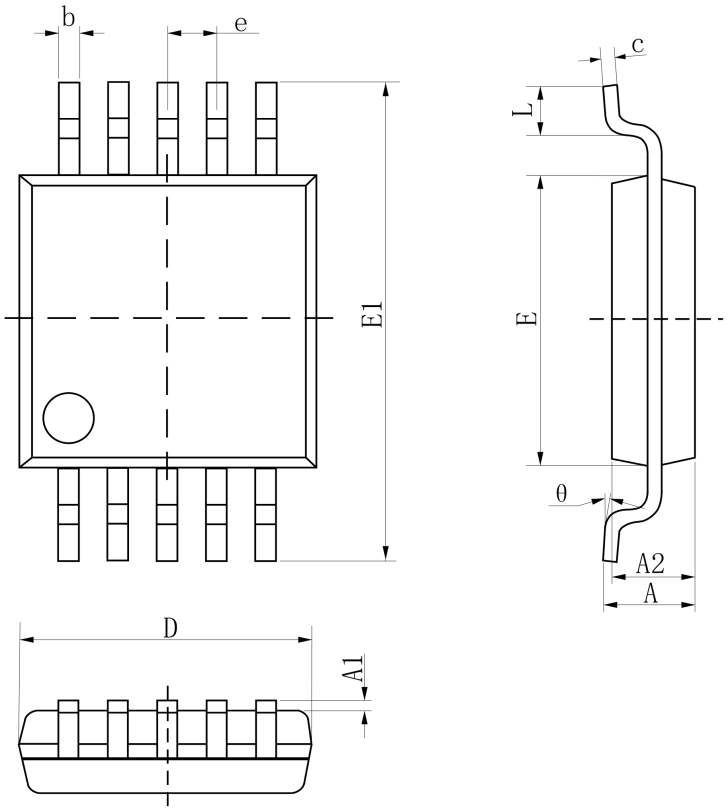


Figure 8. Low-side Current Measurement

PACKAGE OUTLINE DIMENSIONS

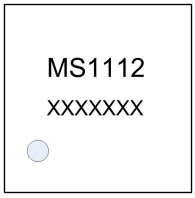
MSOP10



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.50BSC		0.020BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description



Product Name : MS1112

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS1112	MSOP10	3000	1	3000	8	24000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com