TEXAS INSTRUMENTS
TL103W, TL103WA, TL103WB
ZHCSS29R – APRIL 2004 – REVISED APRIL 2024

TL103Wx 具有内部基准的双路运算放大器

1 特性

- 全新的 TL103WB 是 TL103W 和 TL103WA 的引脚兼容型升级版本
- 改进了 B 版本放大器的规格：
  - 电源电压范围：3V 至 36V
  - 最大输入失调电压低：±2mV (25°C) 和 ±2.5mV（在整个温度范围内）
  - 增益带宽：1.2MHz
  - 总电源电流：550 µA
  - EMI 抑制：集成射频和 EMI 滤波器
  - 温度范围：-40°C 至 125°C
- 改进了 B 版本基准的规格：
  - 固定 2.5V 基准
  - 严格的容差，最大值为 0.44% (25°C) 和 1.04%（在整个温度范围内）
  - 宽灌电流范围：0.2mA（典型值）至 100mA

2 应用

- 电池充电器
- 开关模式电源
- 线性电压调节
- 数据采集系统
- 精密恒流阱

3 说明

TL103Wx 器件结合了一个双路运算放大器和一个固定电压基准的构建块，两者通常用于开关模式和线性电源的控制电路。OP AMP1 的同相输入在内部连接到固定的 2.5V 基准，而 OP AMP2 是两个输入均未使用的独立放大器。

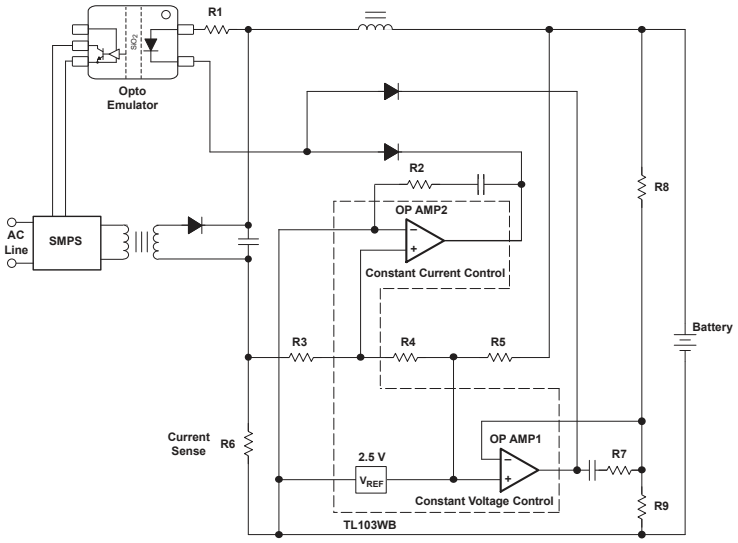
升级的 TL103WB 具有更优的特性，例如更宽的电源电压范围（高达 36V）、更低的电源电流（275 µA/放大器）和更严格的电压调节。这种调节可以通过运算放大器的低失调电压（典型值为 0.3mV）和电压基准的严格容差（25°C 时为 0.44%，运行温度范围内为 1.04%）来实现。

TL103WB 具有 –40°C 至 125°C 的宽温度范围。

封装信息

器件型号	通道数	封装(1)	封装尺寸(2)
TL103W TL103WA	双通道 + 基准	D（SOIC，8）	4.9mm × 6mm
TL103WB		D（SOIC，8）	4.9mm × 6mm
		DDF（SOT-23，8）	2.9mm × 2.8mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



典型应用电路

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4 Pin Configuration and Functions

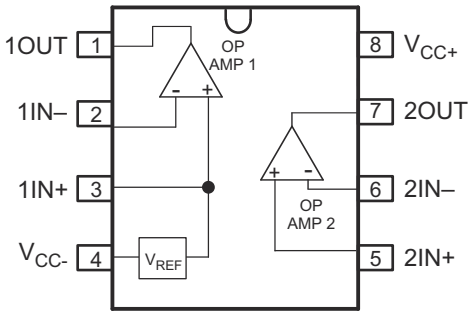

**图 4-1. D and DDF Packages,
8-Pin SOIC and SOT-23-THN
(Top View)**

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OUT	1	O	Opamp 1 output
1IN –	2	I	Opamp 1 inverting input
1IN+	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
V_{CC} –	4	I	Negative Supply Voltage
2IN+	5	I	Opamp 2 non-inverting input
2IN –	6	I	Opamp 2 inverting input
2OUT	7	O	Opamp 2 output
V_{CC+}	8	I	Positive Supply Voltage

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	0	36	V
		TL103WB	0	40	
V_{ID}	Operational amplifier input differential voltage			36	V
V_I	Operational amplifier input voltage range(2)		(V_{CC-}) - 0.3	V_{CC+}	V
I_{KA}	Voltage reference cathode current			100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not applicable to pin 4 (1IN+)

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	3	32	V
		TL103WB	3	36	
V_{ICR}	Input common-mode voltage range		V_{CC-}	(V_{CC+}) - 2	V
I_K	Cathode current	TL103W/TL103WA	0.5	100	mA
		TL103WB	0.2	100	
T_A	Operating free-air temperature	TL103W/TL103WA	–40	105	°C
		TL103WB	–40	125	

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5.4 Thermal Information

THERMAL METRIC[1]		TL103Wx		UNIT
		SOIC (D)	SOT-23 (DDF)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.4	170.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.3	89.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.9	87.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.4	7.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.1	87.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input)

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
AMPLIFIER									
V_{IO}	Input offset voltage	V_{ICM} = 0V		TL103W			±1	±4	mV
					Full range			±5	
				TL103WA			±0.5	±3.0	
					Full range			±5	
				TL103WB			±0.3	±2	
					Full range			±2.5	
αV_{IO}	Input offset-voltage drift			TL103W/TL103WA	Full range		±7		µV/°C
				TL103WB	Full range		±2		
I_{IB}	Input bias current (negative input)			TL103W/TL103WA			-20		nA
				TL103WB			-15		
A_{VD}	Large-signal voltage gain	V_{CC+} = 15V, R_L = 2kΩ, V_{ICM} = 0 V		TL103W/TL103WA			100		V/mV
				TL103WB			210		
PSRR	Supply-voltage rejection ratio	V_{CC+} = 5V to 30V, V_{ICM} = 0V		TL103W/TL103WA		65	100		dB
				TL103WB		99	114		
I_O	Output current	V_{CC+} = 15V, V_O = 2V, V_{ID} = 1V	Source			20	40		mA
			Sink	TL103W/TL103WA		10	12		
				TL103WB		10	24		
		V_{CC+} = 15V, V_O = 0.2V, V_{ID} = -1V	Sink	TL103W/TL103WA		12	50		µA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15V					±40	±68	mA
V_O	Voltage output swing from rail	V_{CC+} = 30V, R_L = 2kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.3		
					Full range	27.4			
		V_{CC+} = 30V, R_L = 10kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
		R_L = 10kΩ	Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15V, C_L = 100pF, R_L = 2kΩ, V_I = 0.5V to 2V, unity gain		TL103W/TL103WA		0.2	0.4		V/µs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103W/TL103WA		0.5[1]	0.9		MHz
		V_{CC+} = 36V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103WB		0.7[1]	1.2		

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5.5 Electrical Characteristics: OP AMP1 (V_{REF} at Noninverting input)（续）

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_{CC+} = 30V, V_O = 2V_{PP}, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB	TL103W/TL103WA			0.02		%
		V_{CC+} = 36V, V_O = 2V_{PP}, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB	TL103WB			0.005		
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5V, no load	TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30V, no load		Full range			2	
		V_{CC+} = 5V, no load	TL103WB			0.55	0.77	
		V_{CC+} = 36V, no load		Full range			1.35	
VOLTAGE REFERENCE								
V_{ref}	Reference Voltage	I_K = 10mA	TL103W		2.482	2.5	2.518	V
				Full Range	2.465		2.535	V
			TL103WA/TL103WB		2.489	2.5	2.511	V
				Full Range	2.474		2.526	V
ΔV_{ref}	Reference input voltage deviation over temperature range	I_K = 10mA	TL103W	Full Range		7	35(1)	mV
			TL103WA/TL103WB	Full Range		7	26(1)	mV
I_{min}	Minimum cathode current for regulation		TL103W/TL103Wx			0.5	1	mA
			TL103WB			0.2	1	
$\|Z_{KA}\|$	Dynamic impedance	I_{KA} = 1mA to 100mA, f < 1kHz				0.45	0.8	Ω

(1) Not tested in production, limits set by characterization and simulation.

5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier)

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{ICM} = 0V	TL103W			±1	±4	mV
				Full range			±5	
			TL103WA			±0.5	±3.0	
				Full range			±5	
			TL103WB			±0.3	±2	
				Full range			±2.5	
αV_{IO}	Input offset-voltage drift		TL103W/TL103WA	Full range		±7		µV/°C
			TL103WB	Full range		±2		
I_{IO}	Input offset current		TL103W/TL103WA			±2	±75	nA
				Full range			±150	
			TL103WB			±0.5	±4	
				Full range			±5	
I_{IB}	Input bias current		TL103W/TL103WA			-20	-150	nA
				Full range			-200	
			TL103WB			-15	-35	
				Full range			-50	
A_{VD}	Large-signal voltage gain	V_{CC+} = 15V, R_L = 2kΩ, VO = 1.4V to 11.4V	TL103W/TL103WA		50	100		V/mV
				Full range	25	100		
			TL103WB		77	210		
				Full range	45	210		
PSRR	Supply-voltage rejection ratio	V_{CC+} = 5V to 30V	TL103W/TL103WA		65	100		dB
			TL103WB		99	114		
V_{ICR}	Input common-mode voltage range	V_{CC+} = 30V			V_{CC-}		(V_{CC+}) – 1.5	V
				Full range	V_{CC-}		(V_{CC+}) – 2	

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5.6 Electrical Characteristics: OP AMP2 (Independent Amplifier) （续）

V_{CC+} = 5V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_{CC+} = 30V		TL103W/TL103WA		70	95		dB
					Full range	60			
				TL103WB		93	104		
					Full range	70			
I_O	Output current	V_{CC+} = 15V, V_O = 2V, V_{ID} = 1V	Source			20	40		mA
			Sink	TL103W/TL103WA		10	12		
				TL103WB		10	24		
		V_{CC+} = 15V, V_O = 0.2V, V_{ID} = -1V	Sink	TL103W/TL103WA		12	50		μA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15V					±40	±68	mA
V_O	Voltage output swing from rail	V_{CC+} = 30V, R_L = 2kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.3		
					Full range	27.4			
		V_{CC+} = 30V, R_L = 10kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
		R_L = 10kΩ	Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15V, C_L = 100pF, R_L = 2kΩ, V_I = 0.5V to 2V, unity gain		TL103W/TL103WA		0.2	0.4		V/μs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103W/TL103WA		0.5(1)	0.9		MHz
		V_{CC+} = 36V, V_I = 10mV, C_L = 100pF, R_L = 2kΩ, f = 100kHz		TL103WB		0.7(1)	1.2		
THD	Total harmonic distortion	V_{CC+} = 30V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB		TL103W/TL103WA			0.02		%
		V_{CC+} = 36V, V_O = $2V_{PP}$, C_L = 100pF, R_L = 2kΩ, f = 1kHz, A_V = 20dB		TL103WB			0.005		
V_n	Equivalent input noise voltage	V_{CC+} = 30V, R_S = 100 Ω, f = 1kHz		TL103W/TL103WA			50		nV/√Hz
		V_{CC+} = 36V, R_S = 100 Ω, f = 1kHz		TL103WB			38		
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5V, no load		TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30V, no load			Full range			2	
		V_{CC+} = 5V, no load		TL103WB			0.55	0.77	
		V_{CC+} = 36V, no load			Full range			1.35	

(1) Not tested in production, limits set by characterization and simulation.

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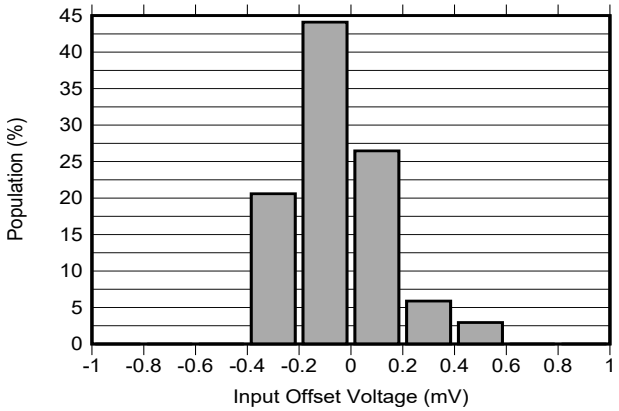
5.7 Typical Characteristics: TL103WB

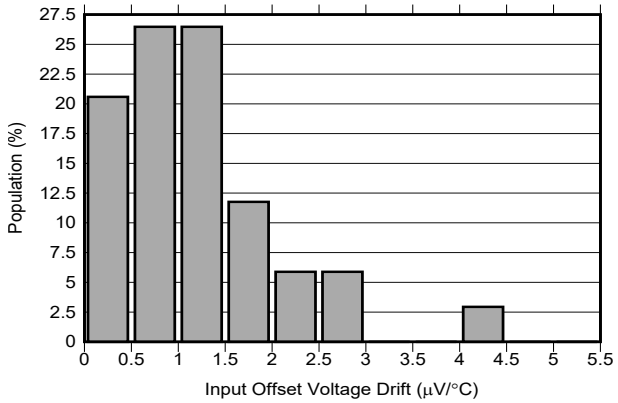
at $T_A \cong 25°C$, V_{CC} = 36V (±18V), $V_{CM} = V_{CC} / 2$, R_L = 10kΩ connected to $V_{CC} / 2$ (unless otherwise noted)



V_{CC} = 5V, No. of devices = 34

μ = 61.4 μV, σ = 166.5 μV

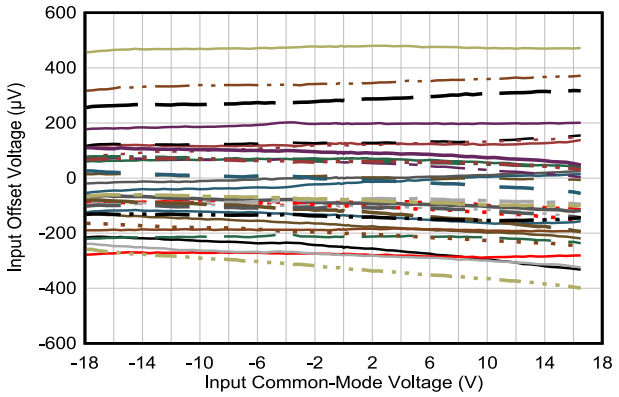
图 5-1. Offset Voltage Distribution Histogram



V_{CC} = 5V, No. of devices = 34

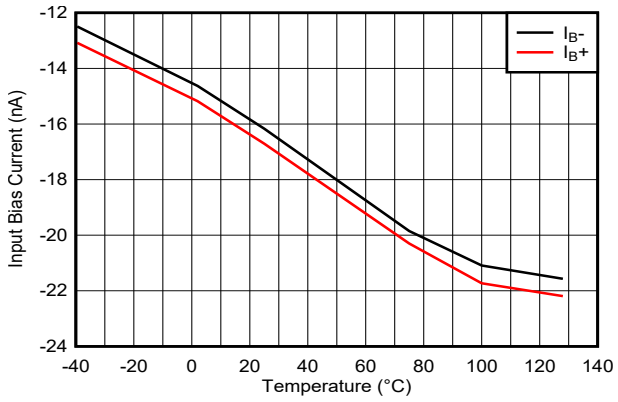
μ = 1.18 μV/°C, σ = 0.81 μV/°C

图 5-2. Offset Voltage Drift Distribution Histogram



No. of devices = 34

图 5-3. Offset Voltage vs Common-Mode



V_{CC} = 5V

图 5-4. Bias Current vs Temperature

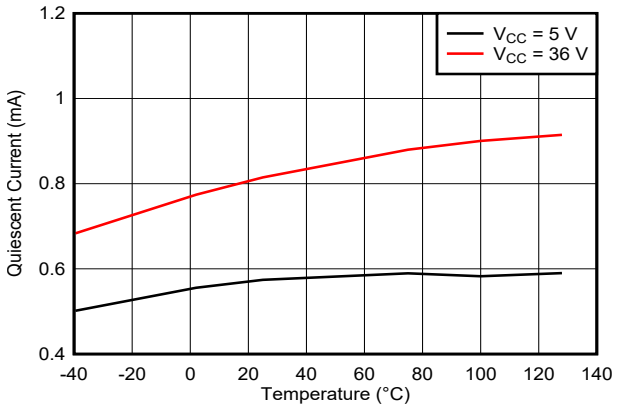
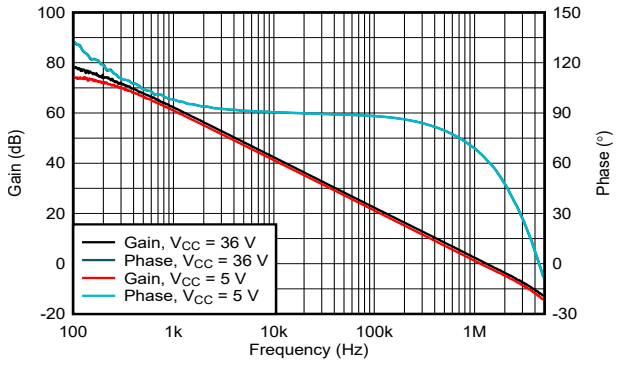


图 5-5. Quiescent Current vs Temperature



R_L = 2kΩ

图 5-6. Open-Loop Gain and Phase vs Frequency

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5.7 Typical Characteristics: TL103WB (continued)

at $T_A \cong 25°C$, V_{CC} = 36V (±18V), $V_{CM} = V_{CC} / 2$, R_L = 10kΩ connected to $V_{CC} / 2$ (unless otherwise noted)

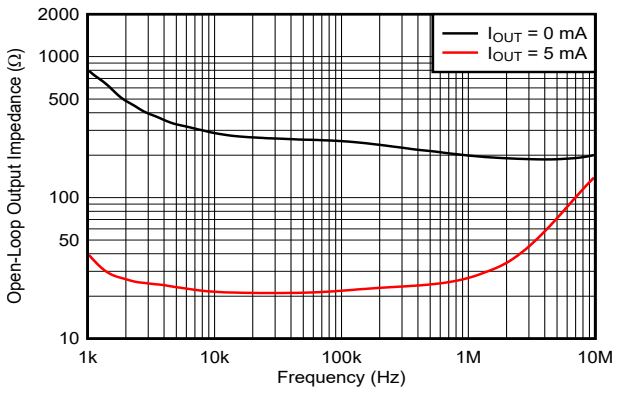


图 5-7. Open-Loop Output Impedance vs Frequency

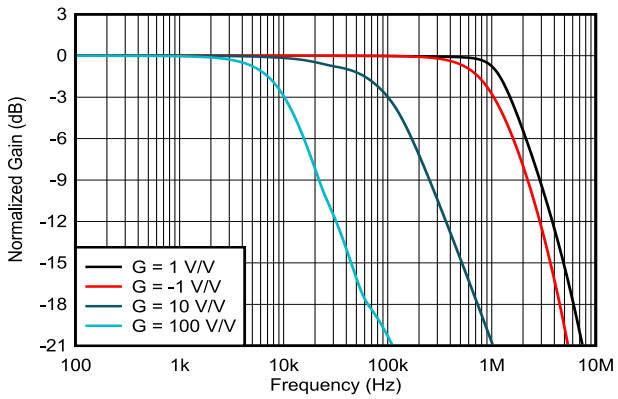


图 5-8. Closed-Loop Gain vs Frequency

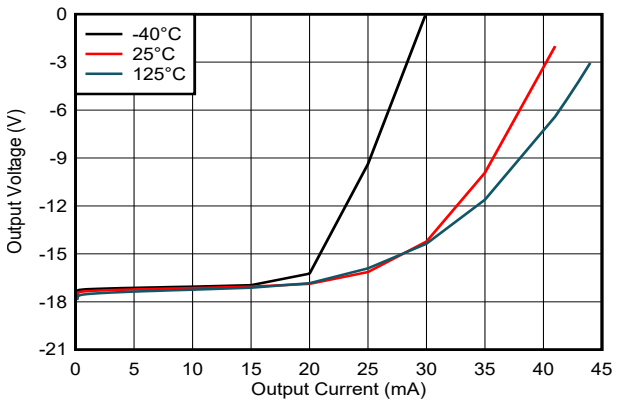


图 5-9. Output Voltage vs Output Current (Sinking)

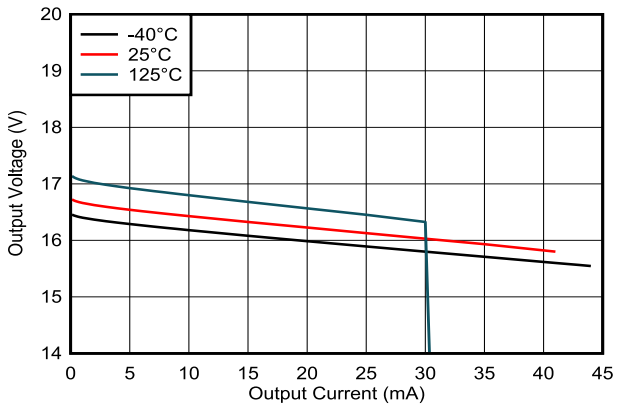


图 5-10. Output Voltage vs Output Current (Sourcing)

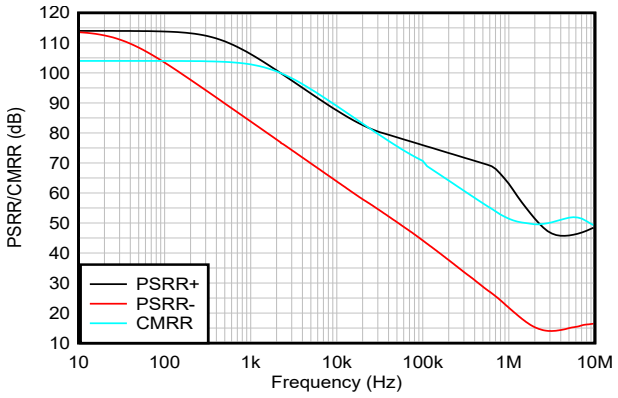
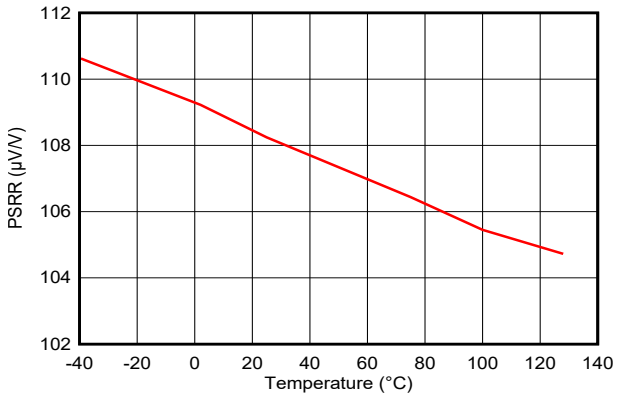


图 5-11. PSRR and CMRR vs Frequency



V_{CC} = 5V to 36V

图 5-12. Supply-Voltage Rejection Ratio vs Temperature

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5.7 Typical Characteristics: TL103WB (continued)

at $T_A \cong 25°C$, V_{CC} = 36V (±18V), $V_{CM} = V_{CC} / 2$, R_L = 10kΩ connected to $V_{CC} / 2$ (unless otherwise noted)

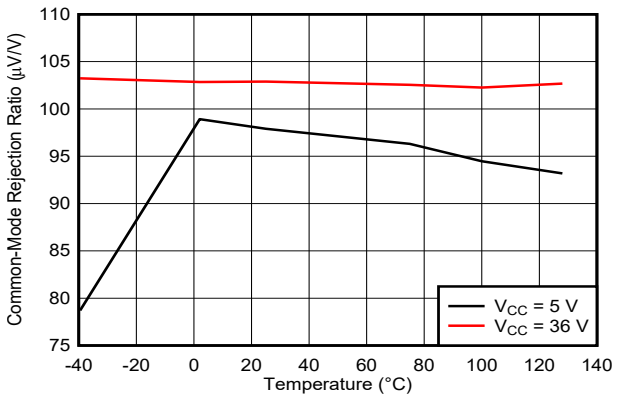


图 5-13. CMRR vs Temperature

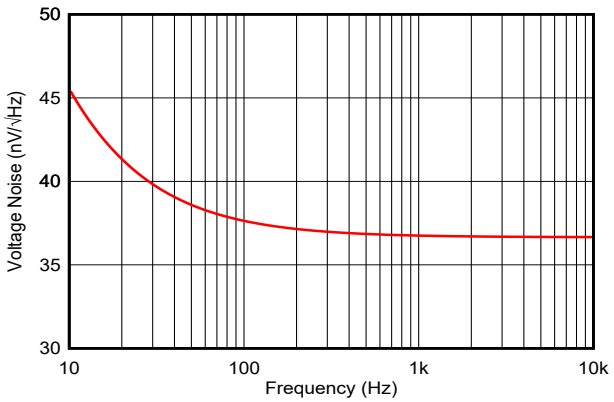
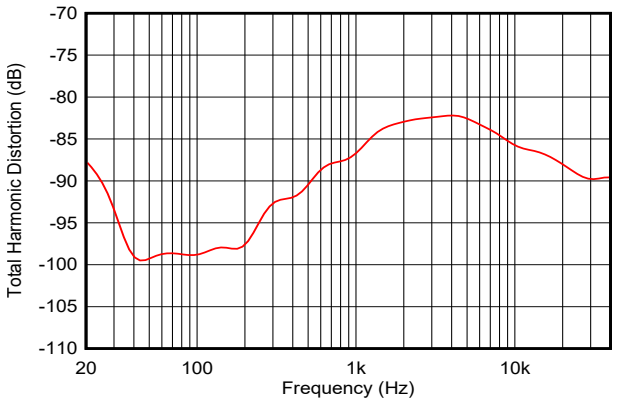
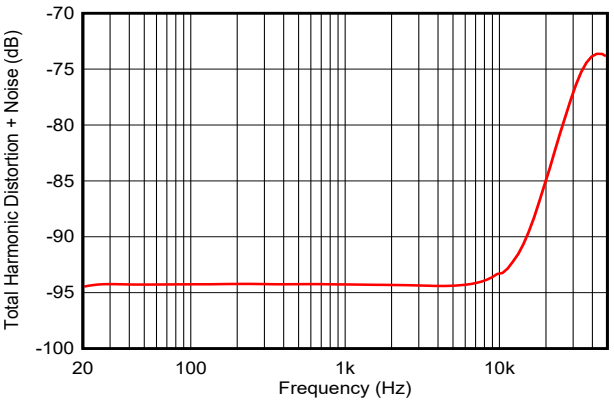


图 5-14. Input Voltage Noise Spectral Density vs Frequency



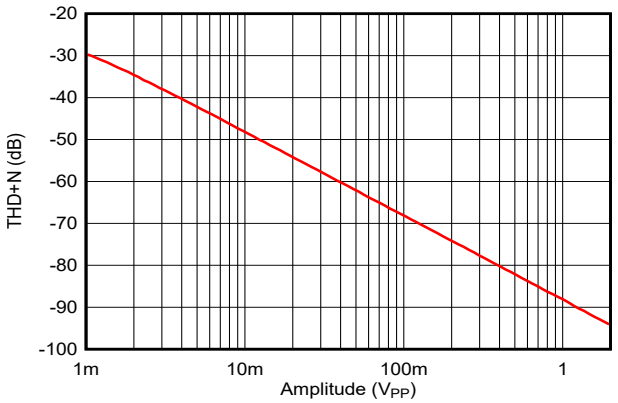
V_{CC} = 30V, V_{OUT} = $2V_{PP}$, R_L = 2kΩ, C_L = 100pF, A_V = 20dB

图 5-15. Total Harmonic Distortion vs Frequency



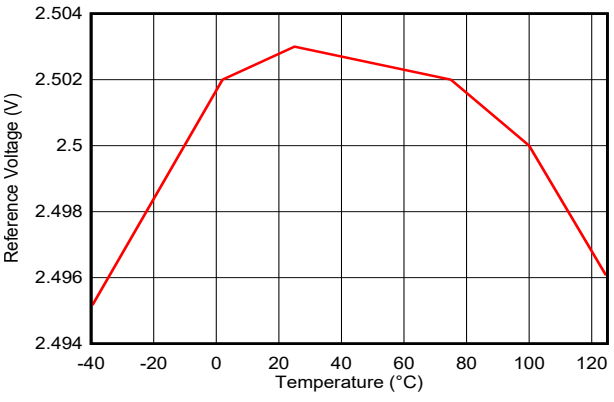
V_{OUT} = $2V_{PP}$, R_L = 2kΩ, BW = 80kHz, A_V = 0dB

图 5-16. Total Harmonic Distortion + Noise vs Frequency



f = 1kHz, R_L = 2kΩ, BW = 80kHz, A_V = 0dB

图 5-17. Total Harmonic Distortion + Noise vs Amplitude



V_{CC} = 5V, I_K= 10 mA

图 5-18. Reference Voltage vs Temperature

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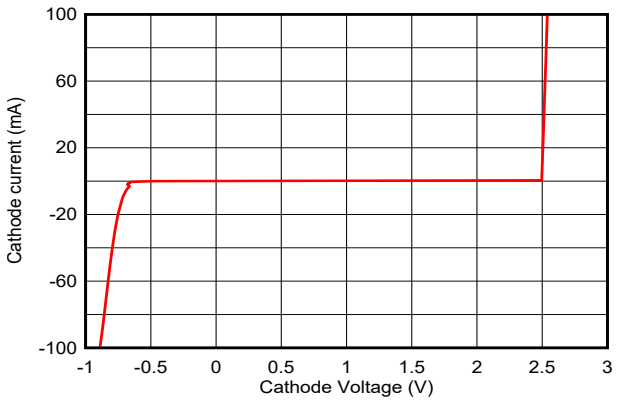
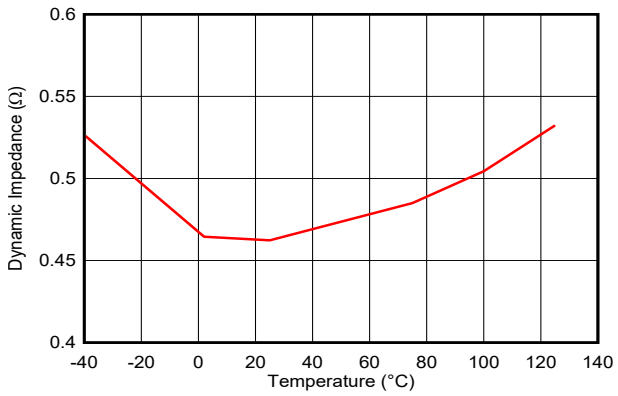
5.7 Typical Characteristics: TL103WB (continued)

at $T_A \cong 25°C$, V_{CC} = 36V (±18V), $V_{CM} = V_{CC} / 2$, R_L = 10kΩ connected to $V_{CC} / 2$ (unless otherwise noted)



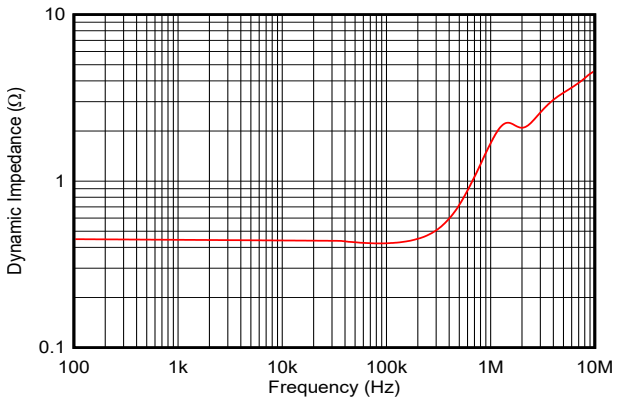
V_{CC} = 5V

图 5-19. Cathode Current vs Cathode Voltage



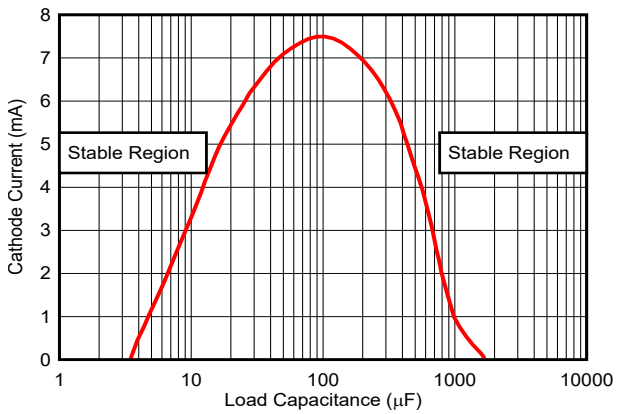
V_{CC} = 5V

图 5-20. Reference Dynamic Impedance vs Temperature



V_{CC} = 5V, I_K = 10 mA

图 5-21. Reference Dynamic Impedance vs Frequency



The area under the curve represents typical conditions that can cause the device to oscillate

图 5-22. Reference Stability vs Capacitive Load

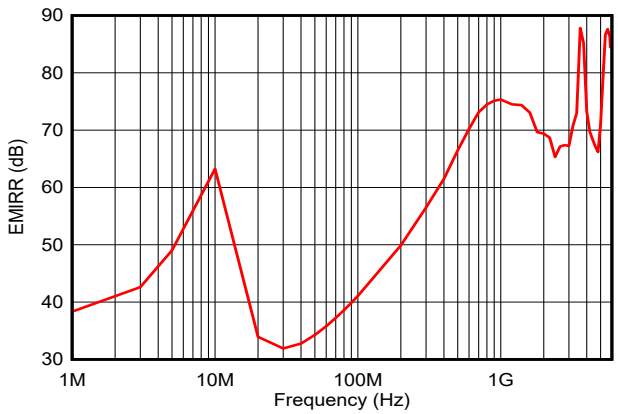


图 5-23. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

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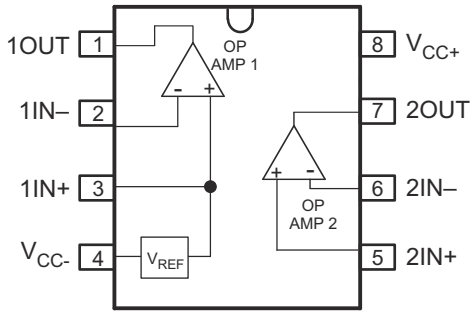
6 Detailed Description

6.1 Overview

The TL103Wx features two high-voltage amplifiers and a shunt voltage reference to allow for cost-sensitive and compact battery charger CC/CV feedback circuits. The upgraded TL103WB features is designed to provide a wide supply range (up to 36V), low offset voltage (±0.3mV typical) and a 1.2MHz bandwidth. The integrated voltage reference is tied to the non-inverting pin of one of OP AMP 1 and provides a fixed 2.5V referenced to the negative supply of the device. The shunt reference of the TL103WA/TL103WB features a tight tolerance of 0.44% at 25°C.

When a single supply voltage of 5V is used (or ±2.5V split supply), the TL103Wx internal reference allows for a more accurate and power-efficient mid-supply signal to be used throughout your circuit. The TL103W/TL103WA devices are characterized for operation from -40°C to 85°C, the TL103WB devices are characterized for operation from –40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal Reference

The TL103Wx family features an internal shunt reference, tied to the non-inverting pin of one of the devices amplifiers. When supplied with enough voltage headroom (≥ 2.5V) and cathode current (0.5mA typical), the reference of the TL103Wx is forced to a fixed 2.5V. To not exceed the maximum cathode current, be sure that the reference input is current limited. Unlike many linear regulators, the reference of the TL103W is internally compensated to be stable without an output capacitor between the cathode and anode. If the reference is used to supply a load, stability criteria shown in 图 5-22 needs to be met.

Reference voltage tolerance varies based off the device grade chosen. At 25°C the TL103W features a reference tolerance of 0.72%, while the TL103WA/TL103WB both feature reference tolerances of 0.44%.

6.3.2 Input Common Mode Range

The valid common mode range is from device ground to V_{CC+} – 1.5V (V_{CC+} – 2V across temperature). Inputs may exceed V_{CC+} up to the absolute maximum voltage without device damage. At least one input must be in the valid input common-mode range for the output to be the correct phase. If both inputs exceed the valid range, then the output phase is undefined. If either input is more than 0.3V below V_{CC-} then input current should be limited to 1mA and the output phase is undefined.

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6.3.3 EMI Rejection

The TL103WB uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications (radio frequency interference - RFI) and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TL103WB benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 图 6-1 shows the results of this testing on the TL103WB. 表 6-1 shows the EMIRR IN+ values for the TL103WB at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

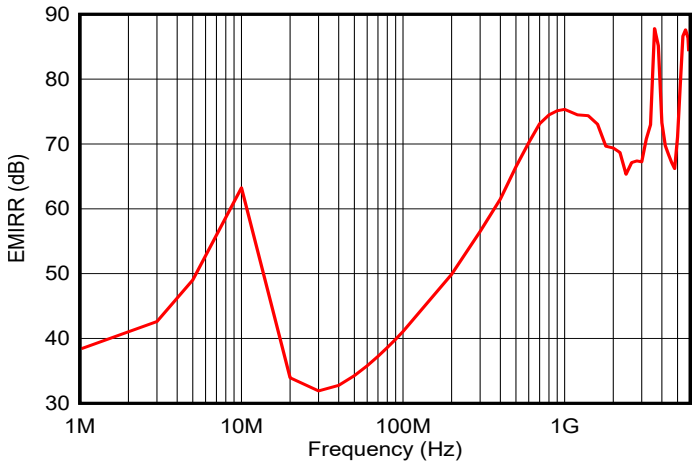

图 6-1. EMIRR Testing

表 6-1. TL103WB EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	62dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	75dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2GHz)	70dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	65dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	71dB

6.4 Device Functional Modes

This device has one mode of operation that applies when operated within the recommended operating conditions.

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7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

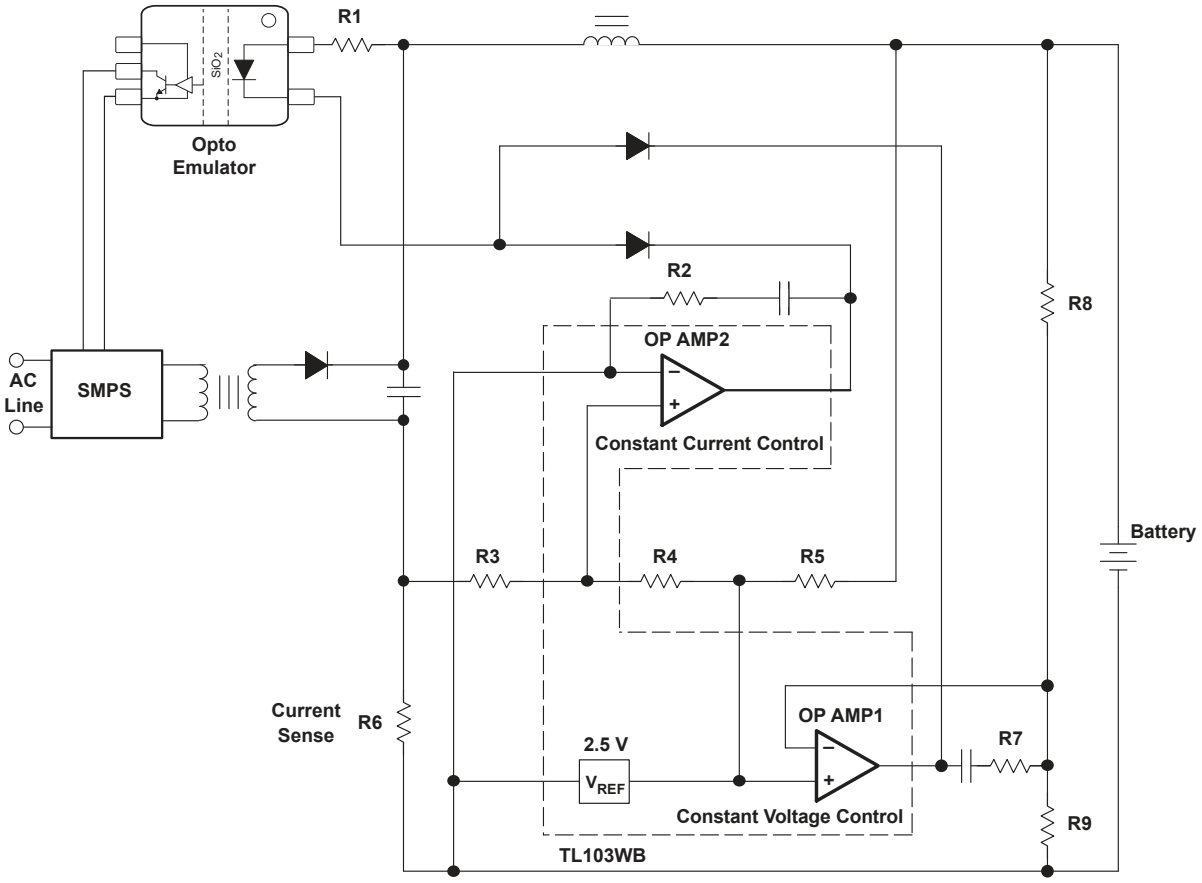
7.1 Application Information

The TL103Wx family offers a cost-effective and compact device for applications requiring both an accurate DC signal and signal conditioning. These devices offer a fixed 2.5V reference, wide bandwidth (1 to 1.2 MHz) and a low total supply current (0.55 to 0.7mA).

7.2 Typical Applications

7.2.1 Isolated Flyback CC/CV Feedback

As shown in 图 7-1, the TL103Wx is often used alongside an opto-coupler/opto-emulator to provide feedback to an isolated flyback. Utilizing the TL103Wx in this way allows for both an accurate and cost-optimized battery charger design that can achieve a stable CC/CV (Constant Current/Constant Voltage) charging profile. In this example, a simplified design procedure will be discussed. Additional details can be found in *Designing CC-CV Feedback Circuits With the TL103WB*.



Typical Application Circuit

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7.2.1.1 Design Requirements

The objective is to design an accurate CC-CV feedback circuit with the requirements provided in 表 7-1.

表 7-1. Design Parameters

PARAMETER	VALUE
Maximum Charge Current	6A
Battery Voltage Range	6V to 20V

7.2.1.2 Detailed Design Procedure

To switch between CV control and CC control, diodes are utilized to achieve an OR logic function as shown in 图 7-1. Designing the circuit in this way allows one of the amplifiers (configured in either CC or CV mode) to dominate the feedback in the design. In this design, *GND* refers to the negative node at the secondary side of the switch-mode power supply.

The fixed 2.5V of the TL103Wx reference provides a stable DC voltage that is used to specify the CC current and CV voltage. One of the requirements of achieving this fixed value, however, is that the cathode of the reference must be supplied with a voltage of 2.5V or above.

7.2.1.2.1 Constant Current Circuit

For the constant current feedback circuit, the amplifier is configured in a low-side current sense configuration. Resistor R6 is used as the current sensing resistor to sense the current flowing between the battery and flyback converter. This is shown in 方程式 1, where I_{BAT} is the output current delivered to the battery. The voltage at the non-inverting input of the amplifier specifies the maximum current (or constant current) that is delivered to the battery.

$$V_{BAT-} = I_{BAT} \times R6 \tag{1}$$

The reference of the TL103Wx is powered by the battery voltage. To be able to achieve a constant current, this reference needs to be provided with 2.5V or greater to provide a fixed 2.5V. The first step in designing a constant current circuit is to specify that 2.5V can be achieved at the battery's minimum voltage. The value of R5 must also be designed so that a sink-current between 0.5mA to 100 mA (for TL103W or TL103WA) is achieved across the specified range of the battery voltage. These two steps are shown below.

$$V_{BAT}(min) \times \frac{R4 + R3}{R4 + R3 + R5 + R6} \geq 2.5\ \text{V} \tag{2}$$

$$0.5\ \text{mA} \leq \frac{\text{V}_{BAT} - V_{REF}}{R5} \leq 100\ \text{mA} \tag{3}$$

For this design R5 is chosen to be 2kΩ. Knowing this and the specified battery range of 6V to 20V, we can calculate that the reference sinks anywhere from 1.75mA to 10mA using 方程式 2.

Once a fixed 2.5V reference is achieved, we can use this accurate DC voltage to specify a constant current target on the non-inverting input of the amplifier. This can be done by calculating the voltage at the amplifier's inverting input when a constant current target is achieved. Specifying R6 to be 10mΩ along with a constant current design target of 6A, we find that this voltage to be 60 mV using 方程式 1. The voltage at the non-inverting pin of the amplifier is specified by 方程式 4.

$$V_{IN+} = 2.5\ V \times \frac{R3}{R4 + R3} \tag{4}$$

Using the component values and design targets calculated so far, 方程式 2 and 方程式 4 can be updated to:

$$6\ V \times \frac{R4 + R3}{R4 + R3 + 2\ k\Omega + 10\ m\Omega} \geq 2.5\ \text{V} \tag{5}$$

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$$60\ mV = 2.5\ V \times \frac{R3}{R4 + R3} \tag{6}$$

Using both 方程式 5 and 方程式 6, we calculate that R3 needs to be greater than around 34.28 Ω. Adding additional headroom to this, we can calculate R3 = 36 Ω and R4 = 1464 Ω.

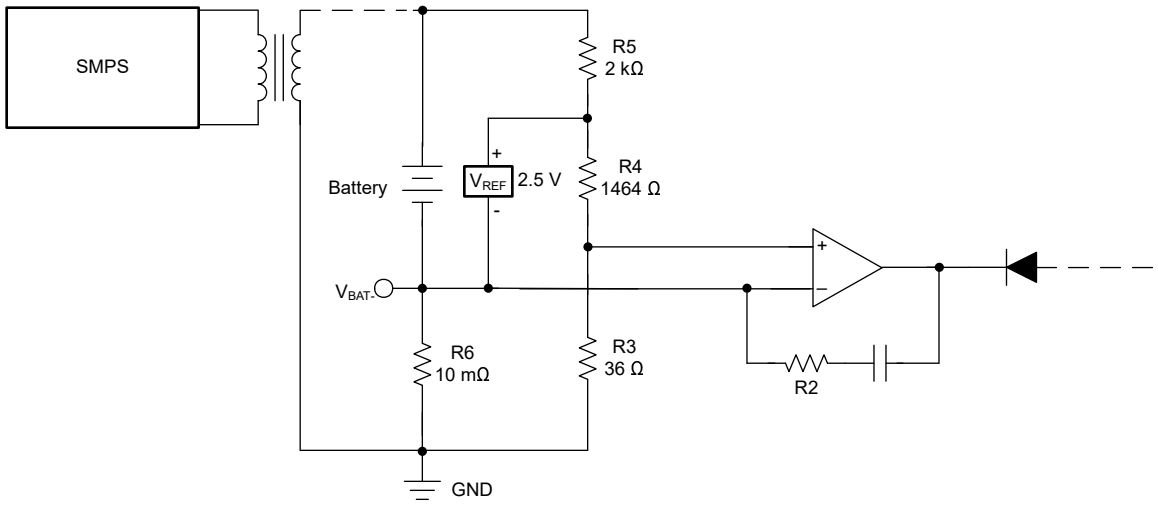

图 7-1. Constant Current Feedback Circuit

7.2.1.2.2 Constant Voltage Circuit

For the constant voltage feedback circuit, resistors R8 and R9 divide down the battery voltage to compare against the TL103Wx's reference. This is shown in 图 7-2. The voltage at the inverting input of the amplifier is designed to equal 2.5V when the battery reaches its maximum specified voltage (or desired constant voltage value). This is shown in for a maximum voltage of 20V provided in 表 7-1.

$$V_{BAT} \times \frac{R9}{R8 + R9} = 2.5\ V \tag{7}$$

$$20\ V \times \frac{R9}{R8 + R9} = 2.5\ V \tag{8}$$

To mimic the constant current circuit and achieve a total impedance and 2k Ω across the battery, R8 is set to 1.96k Ω and R9 to 280 Ω.

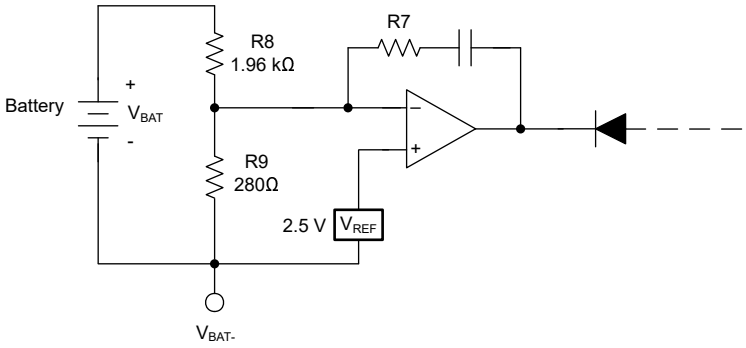

图 7-2. Constant Voltage Circuit

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7.2.2 Constant Current Sink

图 7-3 shows the use of the TL103Wx along with a transistor to provide a constant current sink source. This type of circuit is common in LED drivers and can provide accurate performance and high bandwidth with minimal external components. Accuracy of this circuit is dominated by the reference voltage tolerance, amplifier offset voltage, and resistor tolerance. R_{LIM} is placed to limit the shunt current of the circuit's reference to a maximum of 100mA.

$$I_{SINK} = \left(V_{REF} \times \frac{R_2}{R_1 + R_2}\right) \times R_S \quad (9)$$

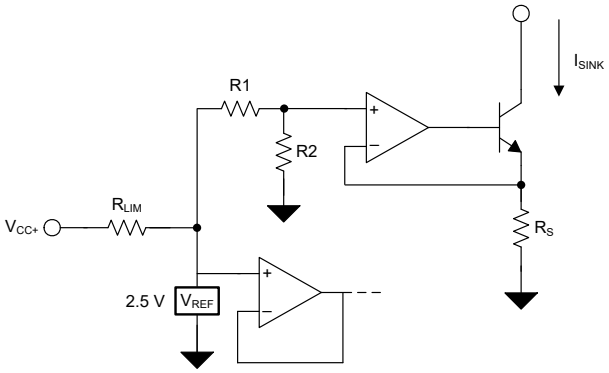

图 7-3. TL103Wx as Constant Current Sink

7.3 Power Supply Recommendations

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 7.4

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - If a bypass capacitor is needed to help stabilize the reference, place this capacitor as close to the reference pin as possible.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If not possible to keep them separate, cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance, as shown in 节 7.4.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

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- For applications shunting high currents through the reference, pay attention to the cathode and anode traces. Ensure the width of these traces are designed with proper current density.

7.4.2 Layout Example

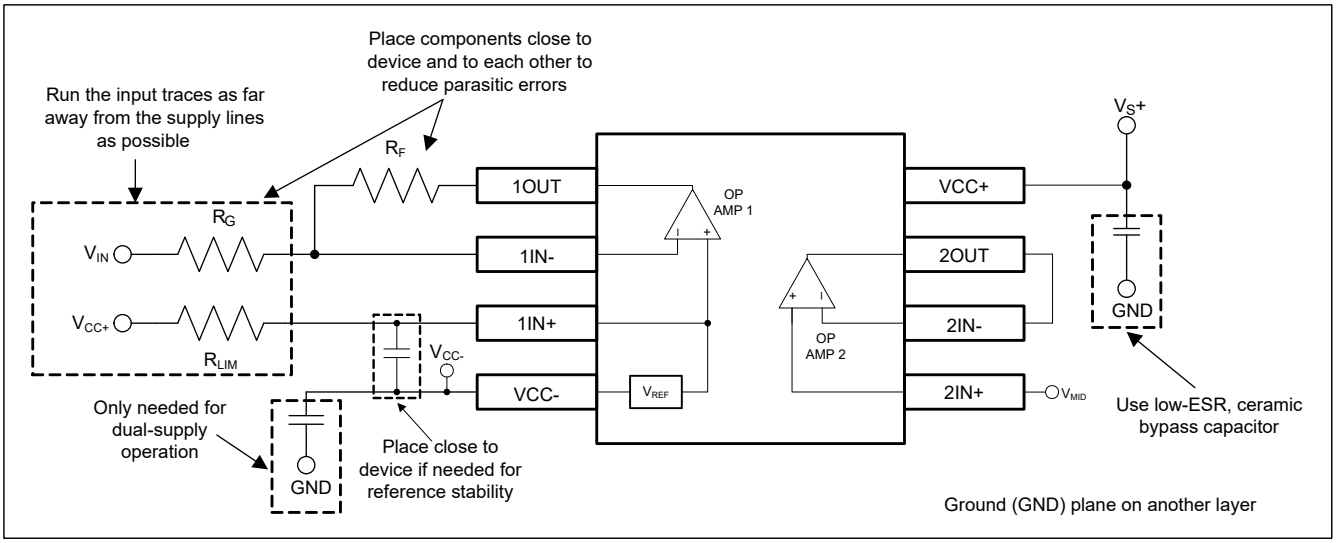

图 7-4. Operational Amplifier Board Layout for Inverting Configuration

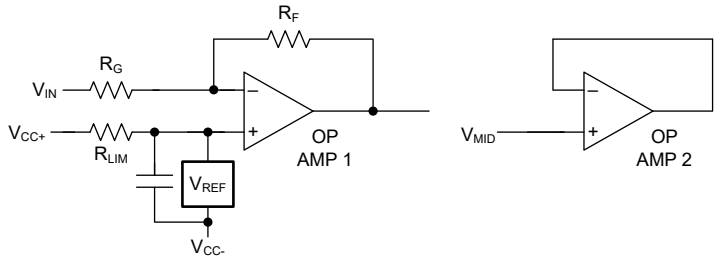

图 7-5. Operational Amplifier Schematic for Inverting Configuration

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
- Texas Instruments, *Designing CC-CV Feedback Circuits With the TL103WB*

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Q (December 2023) to Revision R (April 2024)	Page
• 将 TL103WB DDF (SOT-23, 8) 状态从预告信息（预发布）更改为量产数据（正在供货）	1

Changes from Revision P (November 2023) to Revision Q (December 2023)	Page
• Updated maximum dynamic impedance from 0.5 Ω to 0.8 Ω in *Electrical Characteristics* table	5
• Updated EMIRR IN+ values in *EMIRR IN+ for Frequencies of Interest* table	13

Changes from Revision O (October 2023) to Revision P (November 2023)	Page
• Updated typical large-signal voltage gain of TL103WB from 140V/mV to 210 V/mV	5
• Updated minimum limit of supply-voltage rejection ratio of TL103WB from 80 dB to 99dB	5

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- Added footnote in Electrical Characteristics tables to specify specifications which have limits set by characterization ... 5
- Updated minimum limit of gain bandwidth product for TL103WB from 0.5MHz to 0.7MHz ... 5
- Updated maximum limit of total supply current for TL103WB at 25℃ from 0.92 mA to 0.77mA ... 5
- Updated maximum limit of total supply current for TL103WB at full temperature range from 1.6mA to 1.35mA ... 5
- Updated minimum limit of large-signal voltage gain for TL103WB at 25℃ from 70V/mV to 77V/mV ... 6
- Updated minimum limit of large-signal voltage gain for TL103WB at full temperature range from 35V/mV to 45V/mV ... 6
- Added new CMRR specifications for TL103WB ... 6

Changes from Revision N (August 2023) to Revision O (October 2023) **Page**

- 更改了*特性* 一节中的最大输入失调电压、基准容差、总电源电流和灌电流范围 ... 1
- 更改了*典型应用电路* 图，以包含 TL103WB 和光耦仿真器 ... 1
- 将 TL103WB D（SOIC，8）状态从“预告信息（预发布）”更改为“量产数据（正在供货）” ... 1
- Changed *Thermal Information* table to include latest thermal metrics ... 5
- Added DDF information to *Thermal Information* table ... 5
- Updated k_{SVR} term to PSRR ... 5
- Changed maximum short circuit current from ±60mA to ±68 mA ... 5
- Maximum reference input voltage deviation over temperature range for TL103W was changed from 30mV to 35mV ... 5
- Maximum reference input voltage deviation over temperature range for TL103WA was changed from 30mV to 26mV ... 5
- Added figures to the *Typical Characteristics* section to highlight the TL103WB device ... 8
- Added the *Detailed Description* and *Application and Implementation* sections ... 12
- Added the *Application and Implementation* sections ... 14

Changes from Revision M (October 2016) to Revision N (August 2023) **Page**

- 更新了*特性* 部分，以突出显示 TL103WB ... 1
- 更新了整个文档中的表格、图和交叉参考的编号格式 ... 1
- 通篇添加了 *TL103WB* 器件信息 ... 1
- 更新了*说明* 部分 ... 1
- 更新了*器件信息* 表以包含通道数 ... 1
- Removed DRJ package details and added DDF package for preview ... 3
- Updated formatting for *Electrical Characteristics* tables ... 5
- Updated typical dynamic impedance from 0.2 Ω to 0.45 Ω in *Electrical Characteristics* tables ... 5

Changes from Revision L (February 2016) to Revision M (October 2016) **Page**

- Changed positive and negative terminals OP AMP 2 in the D Package image of *Pin Configuration and Functions* ... 3

Changes from Revision K (October 2010) to Revision L (February 2016) **Page**

- 添加了*器件信息* 表、*引脚配置和功能*、*ESD* 等级、*热性能信息*、*器件和文档支持* 以及*机械、封装和可订购信息* 部分 ... 1

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- 将*特性* 从 2kV ESD 保护 (HBM) 更改为 2.5kV ESD 保护 (HBM)..... 1
- 将*典型应用电路* 中的齐纳二极管元件更改为 V_{REF} 1
- Changed the Zener diode component to V_{REF} in the D Package of *Pin Configuration and Functions* 3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL103WAID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	Z103WA
TL103WAIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA
TL103WAIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA
TL103WBIDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T13DF
TL103WBIDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T13DF
TL103WBIDR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL103D
TL103WBIDR.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL103D
TL103WBIDR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TL103WID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	Z103W
TL103WIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W
TL103WIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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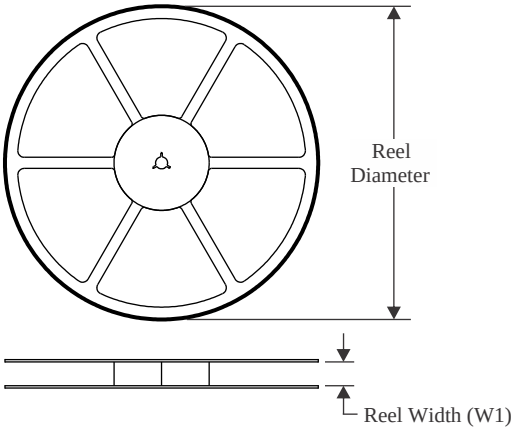
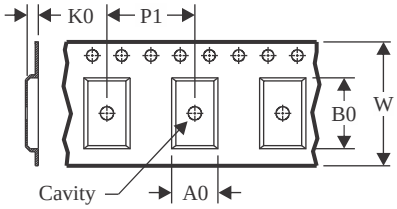
TAPE AND REEL INFORMATION

REEL DIMENSIONS

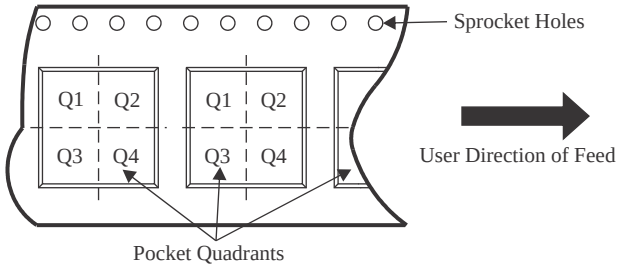


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

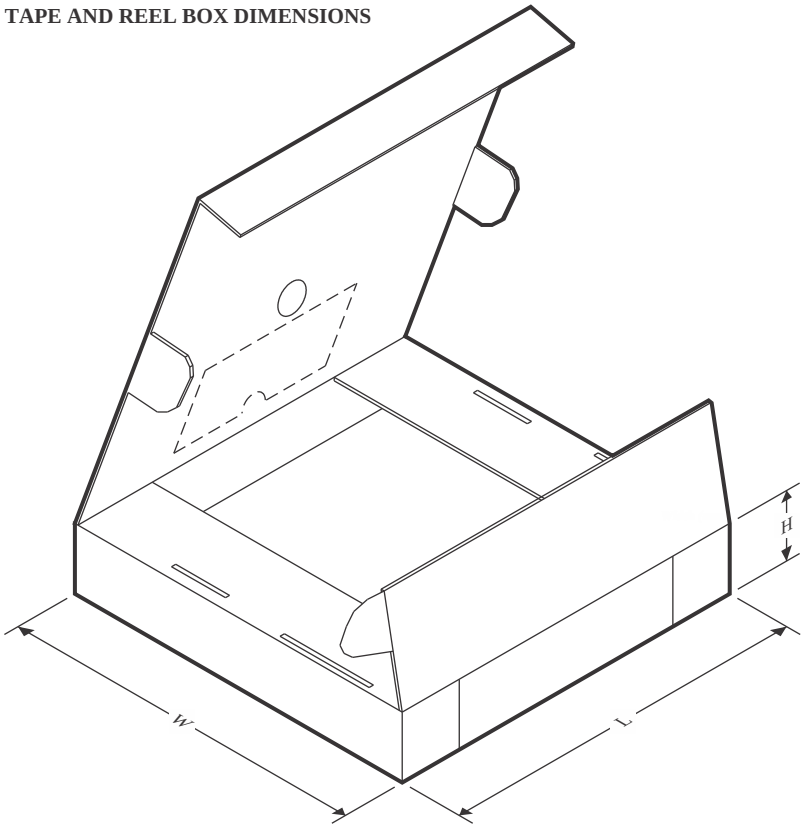
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WBIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL103WBIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

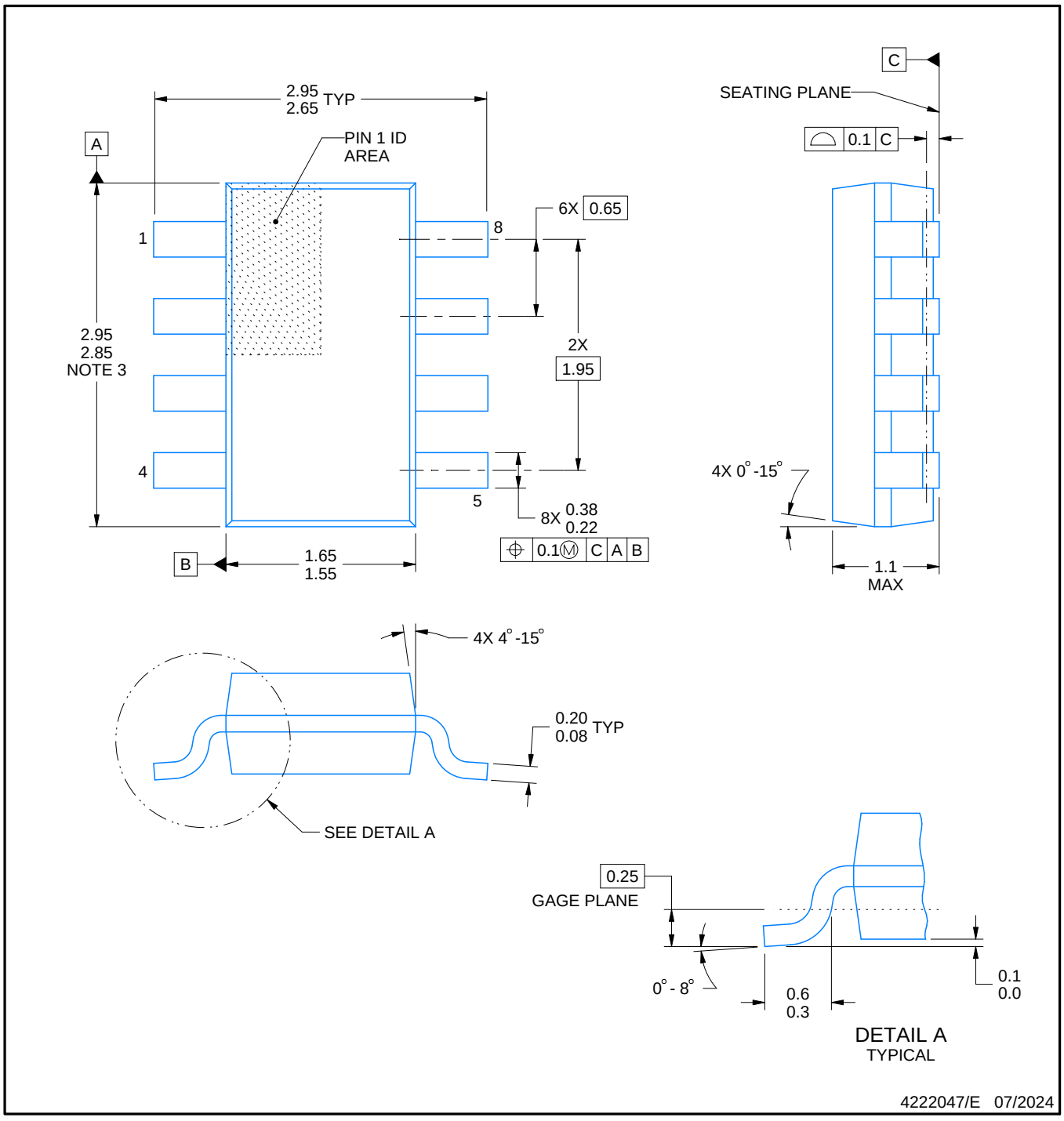
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL103WBIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL103WBIDR	SOIC	D	8	3000	353.0	353.0	32.0
TL103WIDR	SOIC	D	8	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DDF0008A

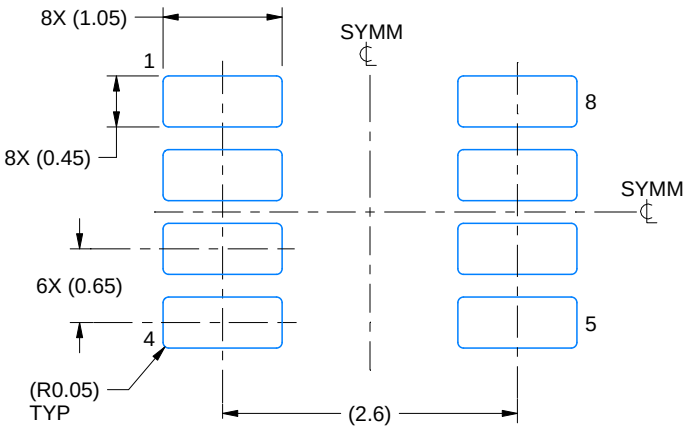
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

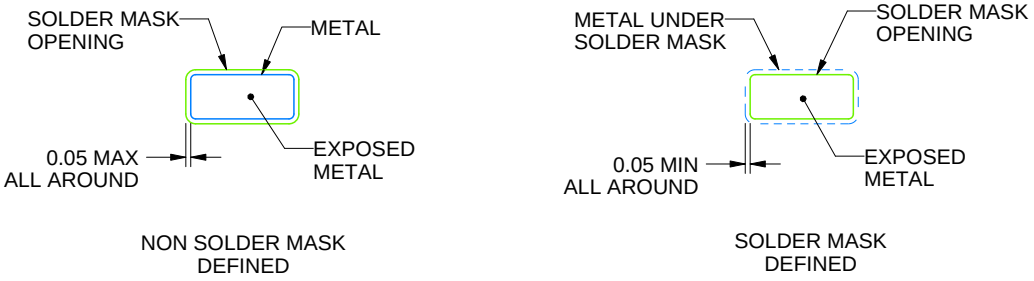


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

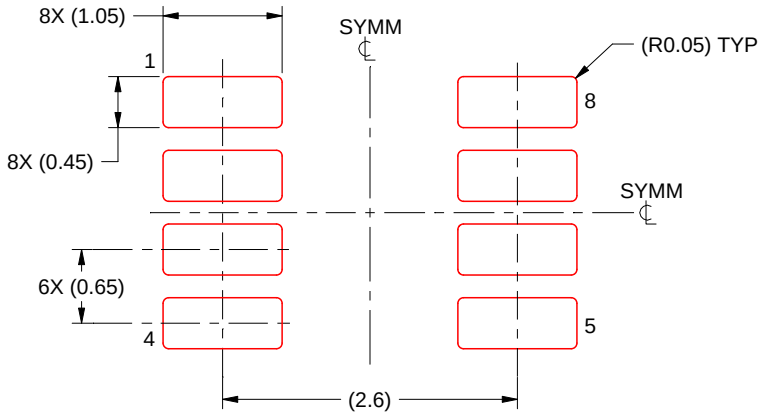


SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

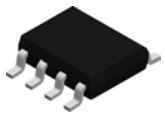


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

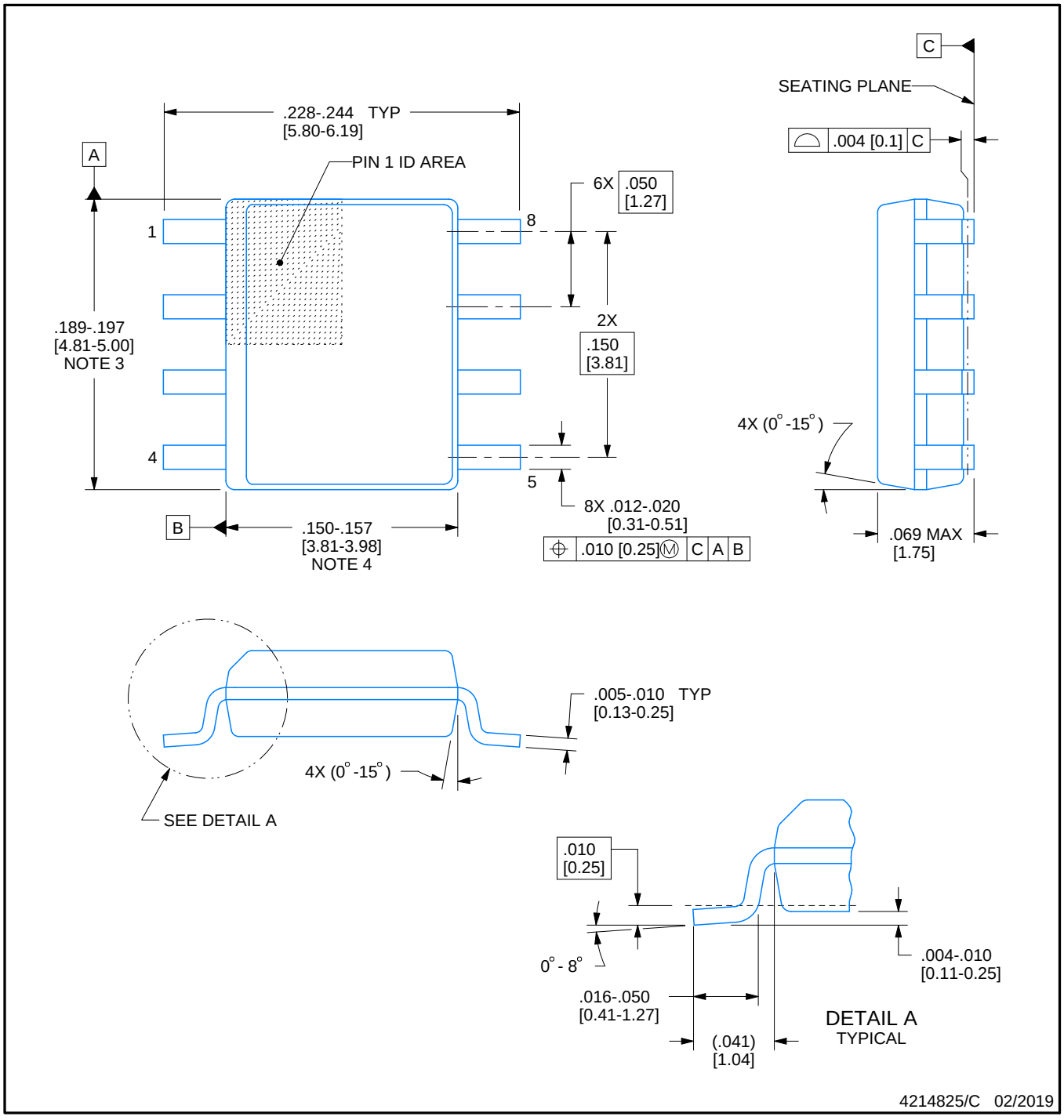


PACKAGE OUTLINE

D0008A

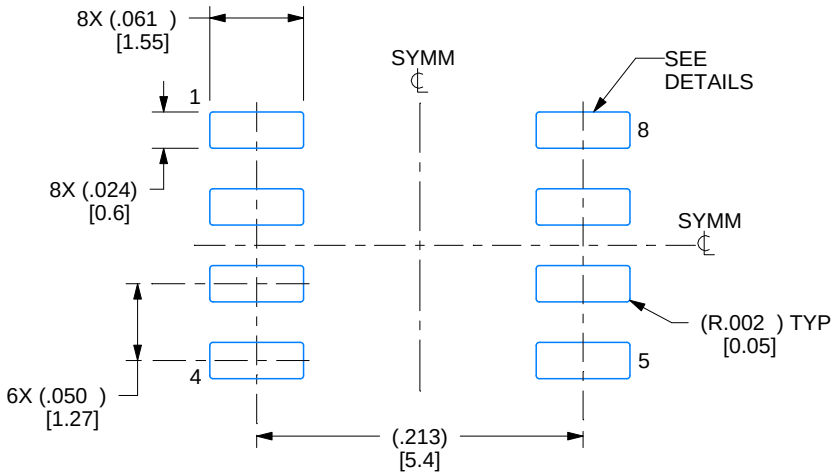
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

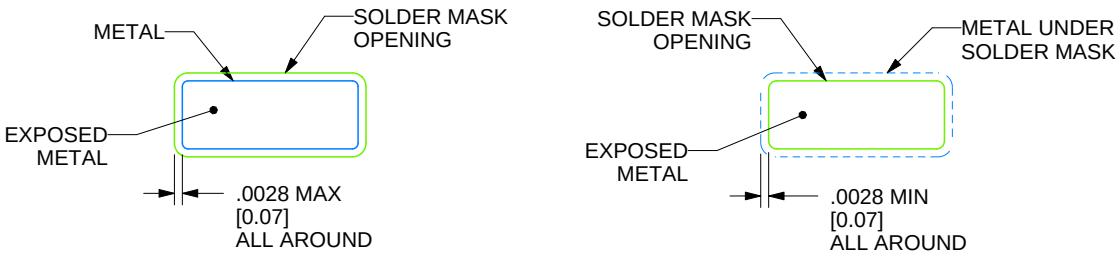


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

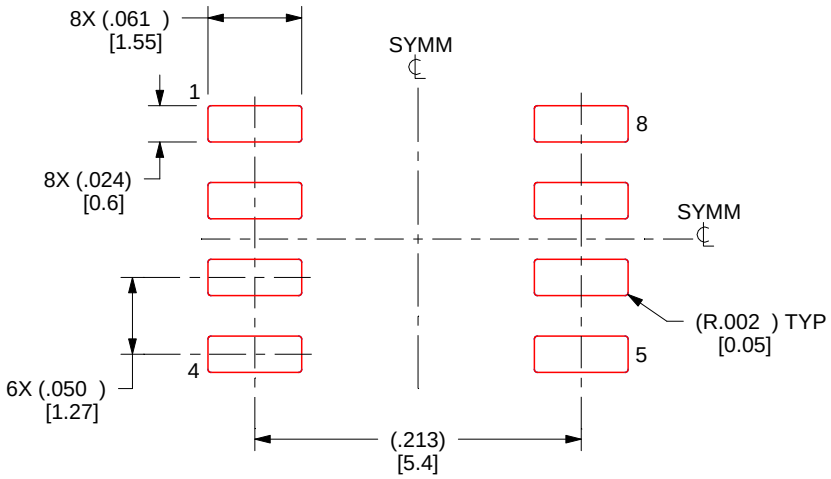
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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