OPA55x High-Voltage, High-Current Operational Amplifiers

1 Features

- Wide Supply Range: ±4 V to ±30 V
- High Output Current: 200 mA Continuous
- Low Noise: 14 nV/√Hz
- Fully Protected:
  - Thermal Shutdown
  - Output Current-Limited
- Thermal Shutdown Indicator
- Wide Output Swing: 2 V from Rail
- Fast Slew Rate:
  - OPA551: 15 V/µs
  - OPA552: 24 V/µs
- Wide Bandwidth:
  - OPA551: 3 MHz
  - OPA552: 12 MHz
- Packages: PDIP-8, SOIC-8, or DDPAK/TO-263-7

2 Applications

- Telephony
- Test Equipment
- Audio Amplifiers
- Transducer Excitation
- Servo Drivers

3 Description

The OPA551x devices are low-cost operational amplifiers with high-voltage (60-V) and high-current (200-mA) capability.

The OPA551 is unity-gain stable and features high slew rate (15 V/µs) and wide bandwidth (3 MHz). The OPA552 is optimized for gains of 5 or greater, and offers higher speed with a slew rate of 24 V/µs and a bandwidth of 12 MHz. Both devices are suitable for telephony, audio, servo, and test applications.

These laser-trimmed, monolithic integrated circuits provide excellent low-level accuracy along with high output swing. High performance is maintained as the amplifier swings to its specified limits.

The OPA55x devices are internally protected against overtemperature conditions and current overloads. The thermal shutdown indicator flag provides a current output to alert the user when thermal shutdown has occurred.

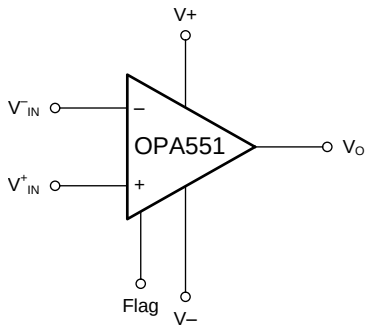
The OPA55x devices are available in PDIP-8 and SOIC-8 packages, as well as a DDPAK-7/TO-263 surface-mount plastic power package. They are specified for operation over the extended industrial temperature range, –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA55x	PDIP (8)	9.81 mm × 6.35 mm
	SOIC (8)	4.9 mm × 3.91 mm
	DDPAK/TO-263 (7)	10.1 mm × 8.99 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Functional Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2003) to Revision B	Page
• Added *ESD Rating* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Changed package references throughout document: *SO-8* to *SOIC-8* and *DDPAK-7* to *DDPAK-7/TO-263*	1
• Deleted lead temperature specifications from *Absolute Maximum Ratings* table	4
• Deleted charged-device model (CDM) specification from *ESD Ratings* table	4

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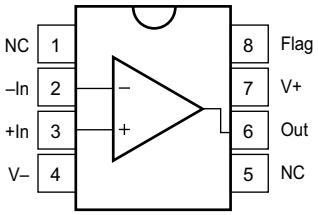
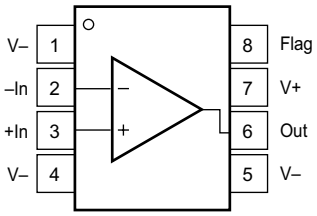
5 Pin Configuration and Functions

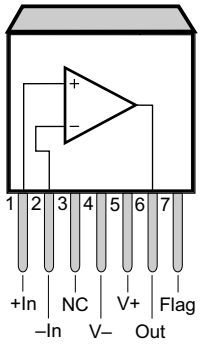
OPA551, OPA552 P Package
8-Pin PDIP
Top View



OPA551, OPA552 D Package
8-Pin SOIC
Top View



OPA551, OPA552 KTW Package
7-Pin DDPAK/TO-263 Surface-Mount
Top View



NOTE: Tab is connected to V– supply.

Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC	PDIP	DDPAK/ TO-263		
Flag	8	8	7	O	Thermal shutdown indicator
+IN	3	3	1	I	Noninverting input
–IN	2	2	2	I	Inverting input
NC	—	1, 5	3	—	No internal connection (can be left floating)
Out	6	6	6	O	Output
Tab	—	—	Tab	—	Connect to V– supply
V+	7	7	5	—	Positive (highest) power supply
V–	1, 4, 5	4	4	—	Negative (lowest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply, V_S = (V+) to (V–)		60	V
Input voltage range, V_{IN}	(V–) – 0.5	(V+) + 0.5	V
Output	See SOA Curve (*Safe Operating Area*)		
Operating temperature, T_A	–55	125	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	8 (±4)	60 (±30)	V
	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA551, OPA552			UNIT
		D (SOIC)	P (PDIP)	KTW (DDPAK/TO-263)	
		8 PINS	8 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.7	44.1	22.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.7	31.8	34.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.2	21.4	7.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	9.1	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.5	21.2	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics: V_S = ±30 V

At T_J = 25°C[1], R_L = 3 kΩ connected to ground, and V_{OUT} = 0 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage		V_{CM} = 0 V, I_O = 0 mA		±1	±3	mV
			T_J = –40°C to 125°C			±5	
dV_{OS} /dT	Input offset voltage vs temperature		T_J = –40°C to 125°C		±7		µV/°C
PSRR	Input offset voltage vs power supply		V_S = ±4 V to ±30 V, V_{CM} = 0 V		10	30	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±20	±100	pA
I_{OS}	Input offset current				±3	±100	pA
NOISE							
e_n	Input voltage noise density		f = 1 kHz		14		nV/√Hz
i_n	Current noise density		f = 1 kHz		3.5		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 2.5		(V+) – 2.5	V
CMRR	Common-mode rejection ratio		–27.5 V < V_{CM} < +27.5 V	92	102		dB
INPUT IMPEDANCE							
	Differential				10^{13} || 2		Ω || pF
	Common-mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain		R_L = 3 kΩ, –28 V < V_O < +28 V	110	126		dB
			R_L = 3 kΩ, –28 V < V_O < +28 V, T_J = –40°C to 125°C	100			
			R_L = 300 Ω, –27 V < V_O < +27 V		120		
OPA551 FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3		MHz
SR	Slew rate		G = 1		±15		V/µs
	Settling time	0.1%	G = 1, C_L = 100 pF, 10-V Step		1.3		µs
		0.01%	G = 1, C_L = 100 pF, 10-V Step		2		
THD+N	Total harmonic distortion + noise		f = 1 kHz, V_O = 15 V_{RMS}, R_L = 3 kΩ, G = 3		0.0005%		
			f = 1 kHz, V_O = 15 V_{RMS}, R_L = 300 kΩ, G = 3		0.0005%		
	Overload recovery time		V_{IN} × Gain = V_S		1		µs
OPA552 FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				12		MHz
SR	Slew rate		G = 5		±24		V/µs
	Settling time	0.1%	G = 5, C_L = 100 pF, 10-V Step		2.2		µs
		0.01%	G = 5, C_L = 100 pF, 10-V Step		3		
THD+N	Total harmonic distortion + noise		f = 1 kHz, V_O = 15 V_{RMS}, R_L = 3 kΩ, G = 5		0.0005%		
			f = 1 kHz, V_O = 15 V_{RMS}, R_L = 300 kΩ, G = 5		0.0005%		
	Overload recovery time		V_{IN} × Gain = V_S		1		µs

(1) All tests are high-speed tested at 25°C ambient temperature. Effective junction temperature is 25°C unless otherwise noted.

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Electrical Characteristics: V_S = ±30 V (continued)

At T_J = 25°C[1], R_L = 3 kΩ connected to ground, and V_{OUT} = 0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Voltage output	I_O = 200 mA	(V–) + 3		(V+) – 3	V
		I_O = 200 mA T_J = –40°C to 125°C	(V–) + 3.5		(V+) – 3.5	
		I_O = 10 mA	(V–) + 2		(V+) – 2	
		I_O = 10 mA T_J = –40°C to 125°C	(V–) + 2.5		(V+) – 2.7	
I_O	Maximum continuous current output: DC	Package dependent — see *Power Dissipation* section	±200			mA
I_{SC}	Short-circuit current			±380		mA
C_{LOAD}	Capacitive load drive	Stable operation	See Figure 19			
SHUTDOWN FLAG						
	Thermal shutdown status output	Normal operation, sourcing		0.05	1	µA
		Thermal shutdown, sourcing	80	120	160	
		Voltage compliance range	V–		(V+) –1.5	V
	Junction temperature	Shutdown		160		°C
		Reset from shutdown		140		
POWER SUPPLY						
V_S	Specified voltage			±30		V
	Operating voltage range		±4		±30	V
I_Q	Quiescent current	I_O = 0 mA		±7	±8.5	mA
		T_J = –40°C to 125°C			±10	
TEMPERATURE RANGE						
T_J	Specified range		–40		125	°C
	Operating range		–55		125	

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6.6 Typical Characteristics

At T_J = 25°C, V_S = ±30 V and R_L = 3 kΩ, unless otherwise noted.

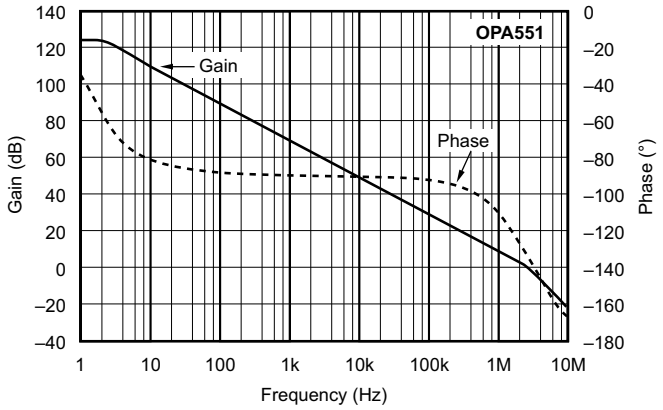

Figure 1. Open-Loop Gain and Phase vs Frequency (OPA551)

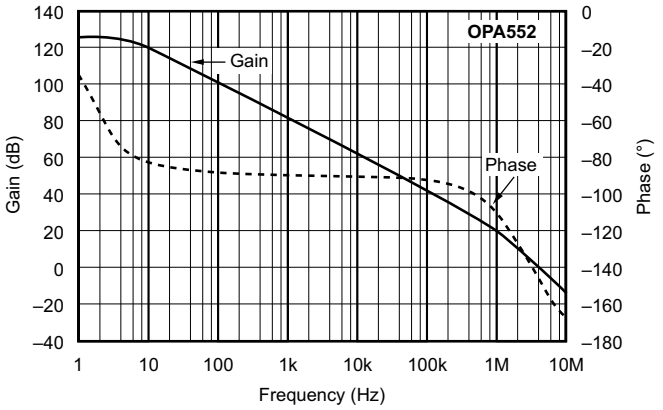

Figure 2. Open-Loop Gain and Phase vs Frequency (OPA552)

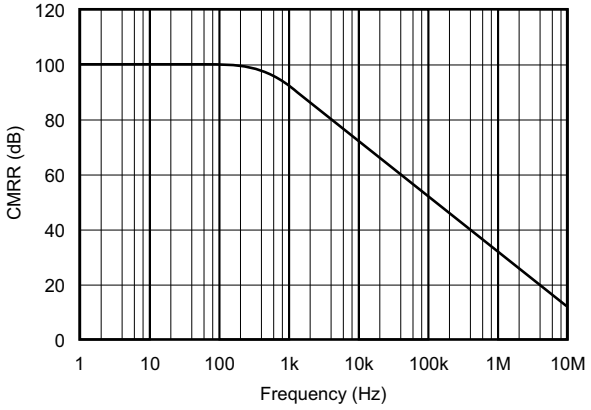

Figure 3. Common-Mode Rejection Ratio vs Frequency

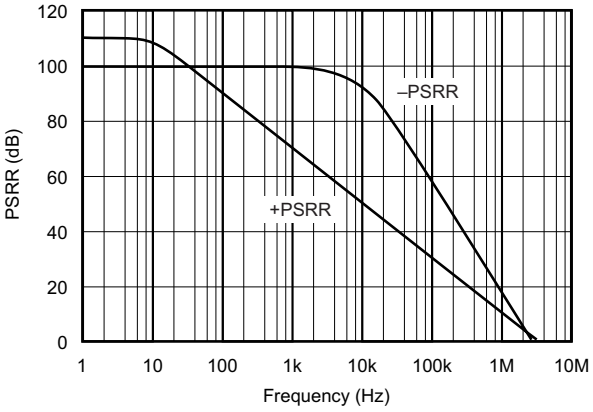

Figure 4. Power-Supply Rejection Ratio vs Frequency

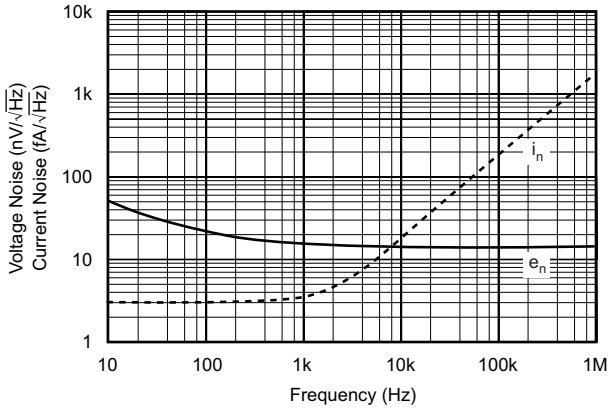

Figure 5. Input Voltage and Current Noise Spectral Density vs Frequency

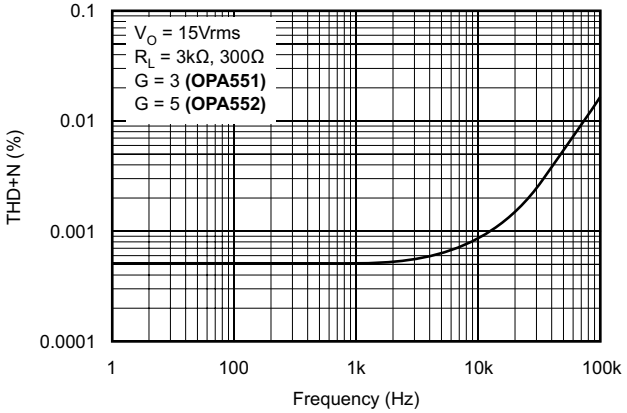

Figure 6. Total Harmonic Distortion + Noise vs Frequency

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Typical Characteristics (continued)

At T_J = 25°C, V_S = ±30 V and R_L = 3 kΩ, unless otherwise noted.

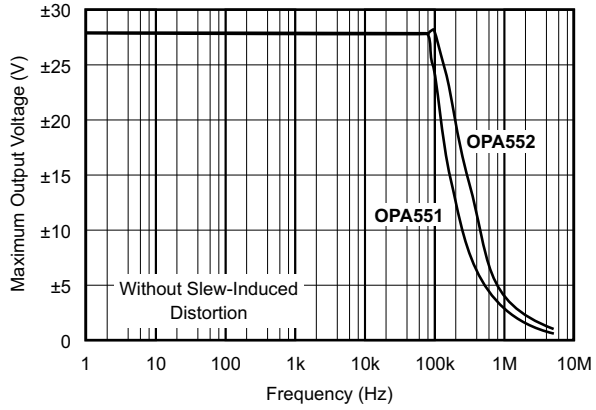

Figure 7. Maximum Output Voltage Swing vs Frequency

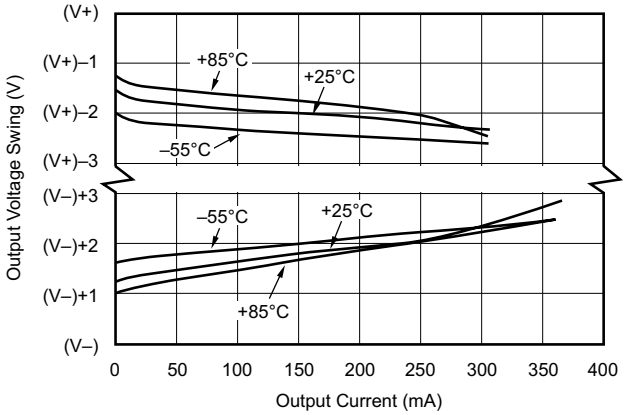

Figure 8. Output Voltage Swing vs Output Current

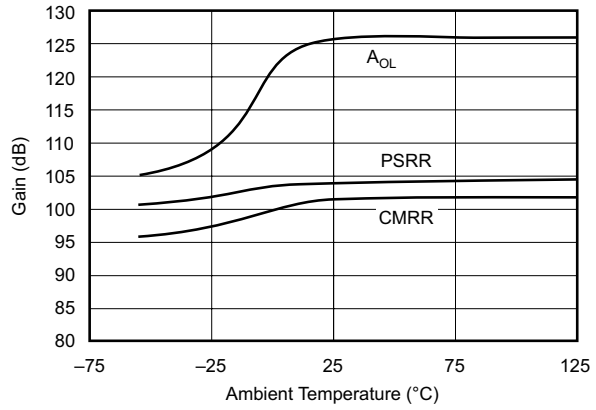

Figure 9. Open-Loop Gain, Power-Supply Rejection Ratio, and Common-Mode Rejection Ratio vs Temperature

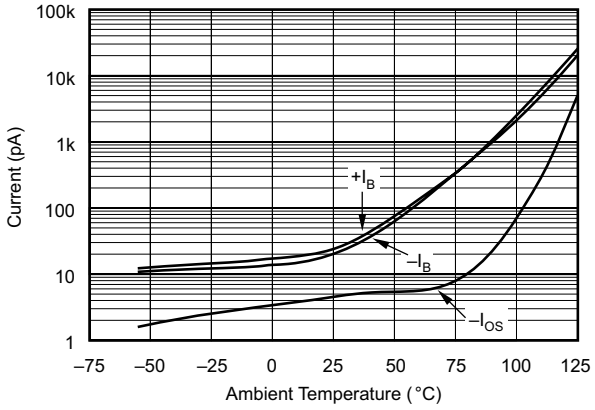

Figure 10. Input Bias Current and Input Offset Current vs Temperature

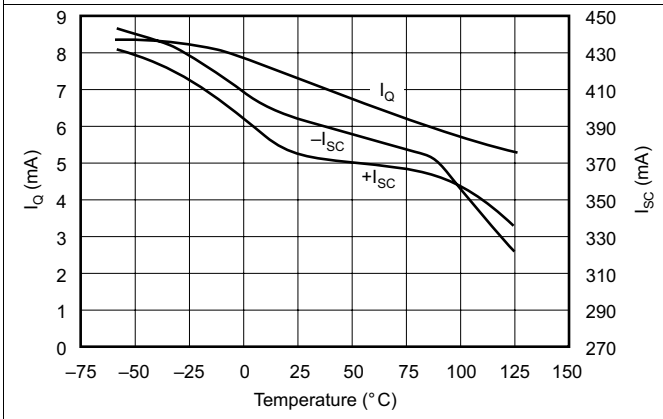

Figure 11. Quiescent Current and Short-Circuit Current vs Temperature

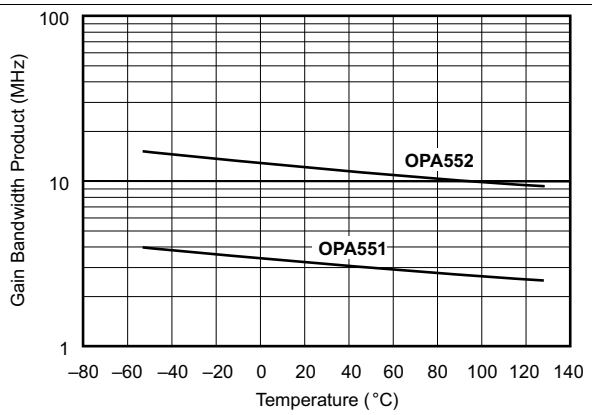

Figure 12. Gain Bandwidth Product vs Temperature

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Typical Characteristics (continued)

At T_J = 25°C, V_S = ±30 V and R_L = 3 kΩ, unless otherwise noted.

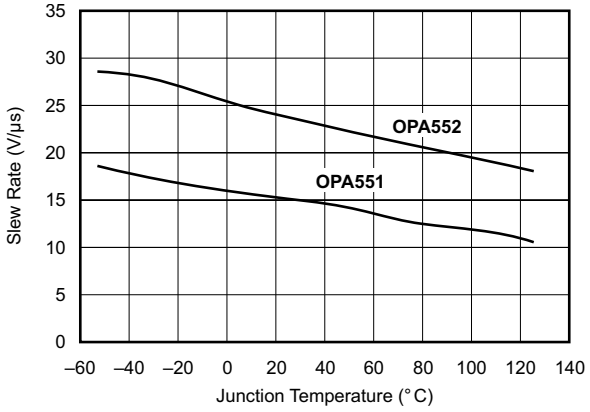


Figure 13. Slew Rate vs Temperature

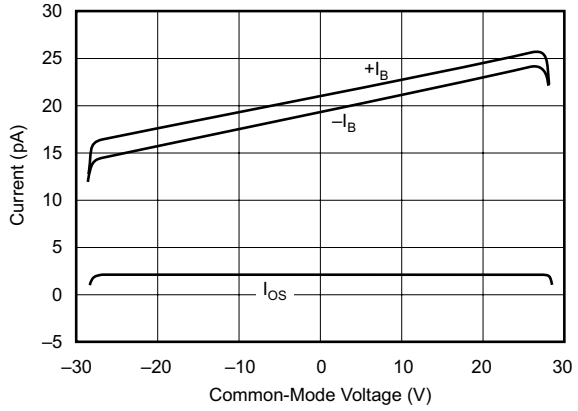


Figure 14. Input Bias Current and Input Offset Current vs Common-Mode Voltage

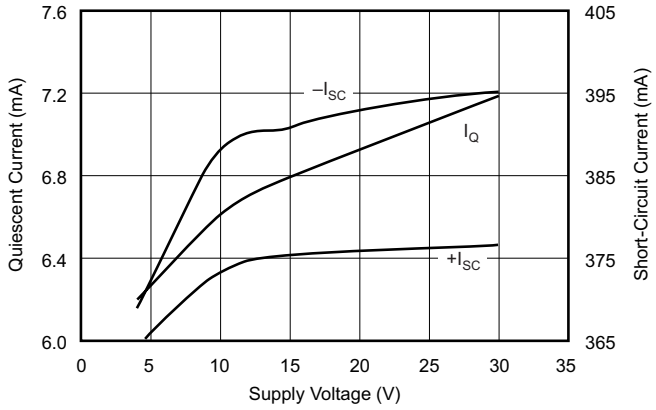


Figure 15. Quiescent Current and Short-Circuit Current vs Supply Voltage

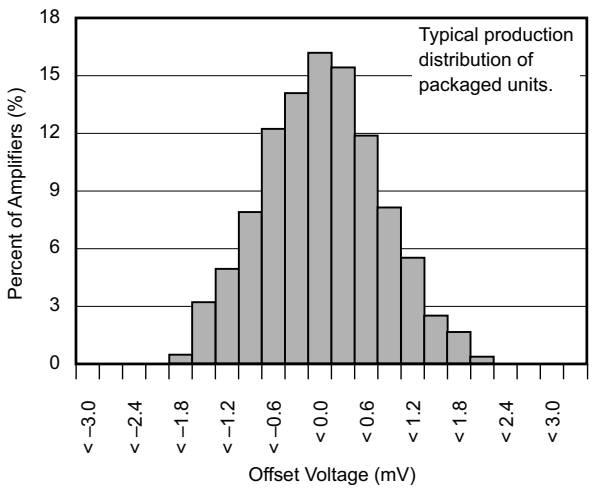


Figure 16. Offset Voltage Production Distribution

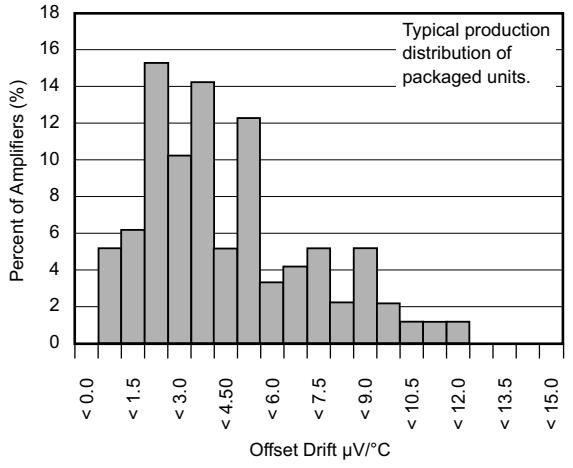


Figure 17. Offset Voltage Drift Production Distribution

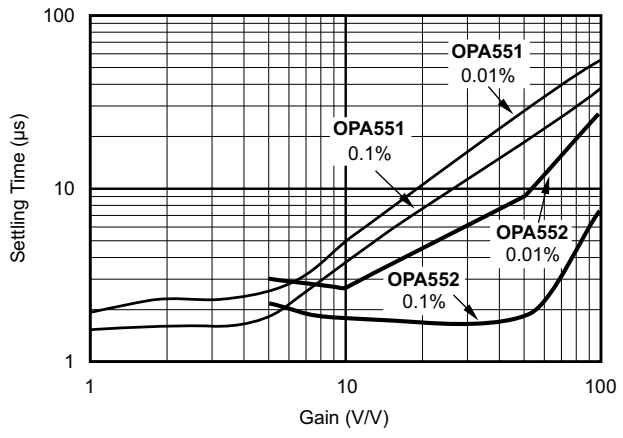


Figure 18. Settling Time vs Closed-Loop Gain

Typical Characteristics (continued)

At T_J = 25°C, V_S = ±30 V and R_L = 3 kΩ, unless otherwise noted.

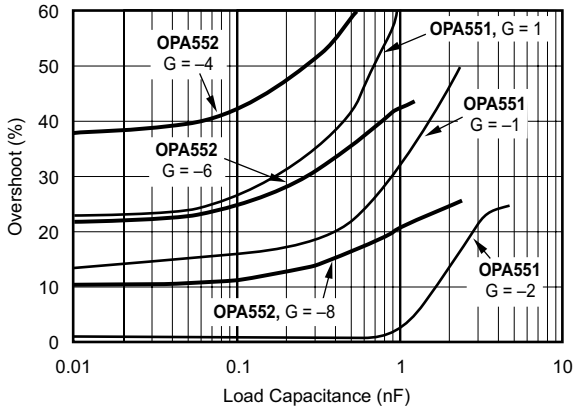
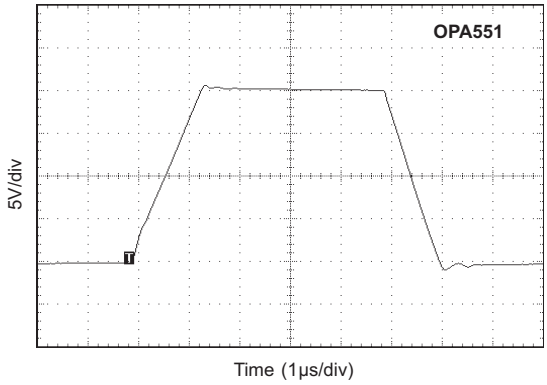
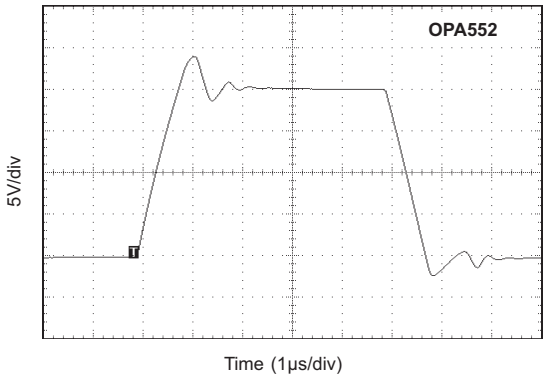


Figure 19. Small-Signal Overshoot vs Load Capacitance



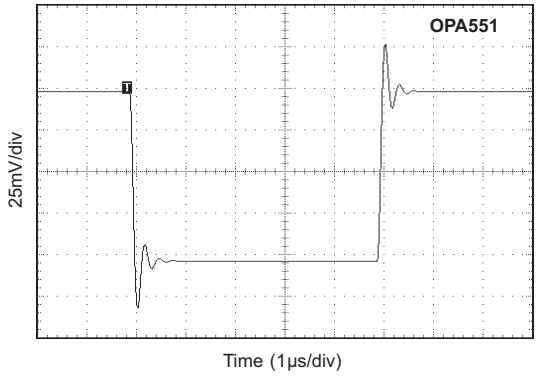
G = 1, C_L = 100 pF

Figure 20. Large-Signal Step Response OPA551



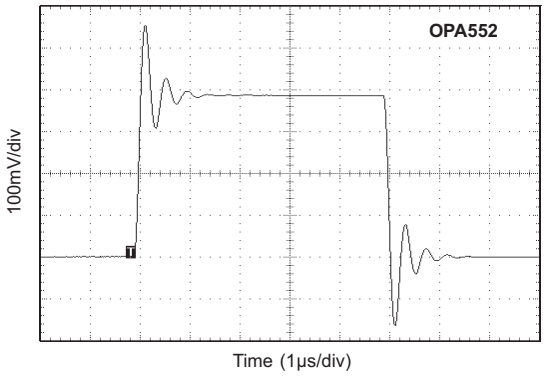
G = 1, C_L = 100 pF

Figure 21. Large-Signal Step Response OPA552



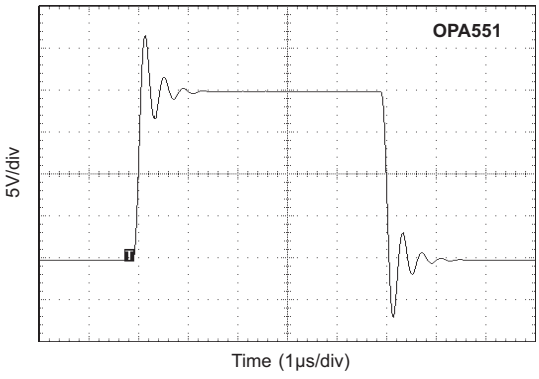
G = 1, C_L = 100 pF

Figure 22. Small-Signal Step Response OPA551



G = 1, C_L = 100 pF

Figure 23. Small-Signal Step Response OPA552



G = 1, C_L = 1000 pF

Figure 24. Small-Signal Step Response OPA551

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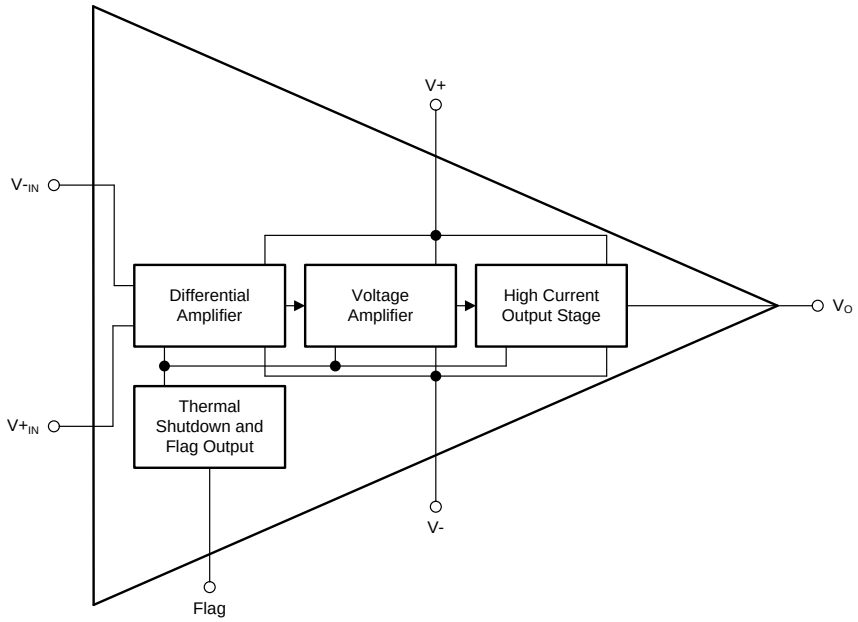
7 Detailed Description

7.1 Overview

The OPA55x devices are low-cost, laser-trimmed, operational amplifiers that feature outstanding low-level accuracy coupled with high output swing. High device performance is maintained as these amplifiers swing to the specified device limits in a wide range of applications. The OPA551 is unity-gain stable while the OPA552 is optimized for gains of 5 or greater.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Thermal Shutdown

Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C and resets when the die has cooled to 140°C. The flag pin can be monitored to determine if shutdown has occurred. During normal operation, the current source from the flag pin is less than 50 nA. During shutdown, the flag pin sources 120 µA (typical).

7.3.2 Current Limit

The OPA55x devices are designed with internal current-limiting circuitry that limits the output current to approximately 380 mA. The current limit varies with increasing junction temperature as shown in (Figure 11). This feature, in combination with the thermal protection circuitry, provides protection from many types of overload conditions, including short-circuit to ground.

7.3.3 Input Protection

The OPA55x features internal clamp diodes to protect the inputs when voltages beyond the supply rails are encountered. However, input current must be limited to 5 mA. In some cases, an external series resistor may be required. Many input signals are inherently current-limited; therefore, a limiting resistor may not be required. Consider that a large series resistor, in conjunction with the input capacitance, can affect stability.

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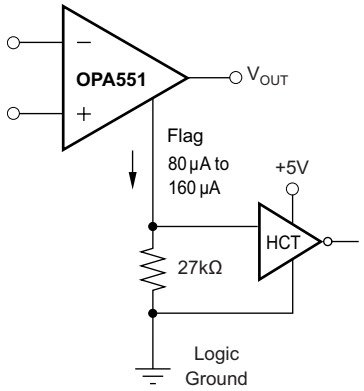
Feature Description (continued)

7.3.4 Thermal Protection

The OPA55x has thermal shutdown circuitry that protects the amplifier from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled.

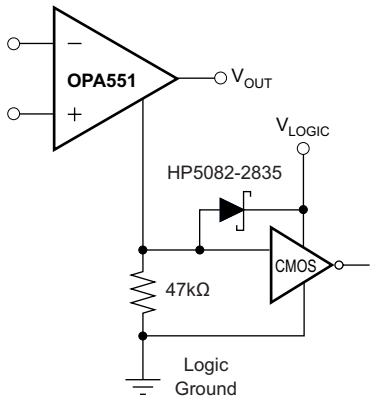
The thermal shutdown function is not intended to replace proper heat sinking. Activation of the thermal shutdown circuitry is an indication of excessive power dissipation or an inadequate heat sink. Continuously running the amplifier into thermal shutdown can degrade reliability.

The thermal shutdown indicator (flag) pin can be monitored to determine if shutdown is occurring. During normal operation, the current output from the flag pin is typically 50 nA. During shutdown, the current output from the flag pin increases to 120 µA (typical). This current output allows for easy interfacing to external logic. Refer to Figure 25 and Figure 26 for two examples that implement this function.



HCT logic has relatively well-controlled logic level. A properly chosen resistor value can ensure proper logic high level throughout the full range of flag output current.

Figure 25. Interfacing With HCT Logic



Interface to virtually any CMOS logic gate by choosing resistor value that provides a guaranteed logic high voltage with the minimum (80 µA) flag current. A diode clamp to the logic supply voltage assures that the CMOS is not damaged by overdrive.

Figure 26. Interfacing With CMOS Logic

7.4 Device Functional Modes

The OPA551 and OPA552 have a single functional mode. The device is operational when the power supply is above 8 V and the junction temperature is below 160°C.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Figure 27 shows the OPA551 connected as a basic noninverting amplifier. The OPA551 can be used in virtually any operational amplifier configuration. The OPA552 is designed for use in configurations with gains of 5 or greater. Power-supply terminals must be bypassed with 0.1-µF capacitors, or greater, near the power-supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used. The OPA55x can supply output currents up to 200 mA with excellent performance.

8.2 Typical Application

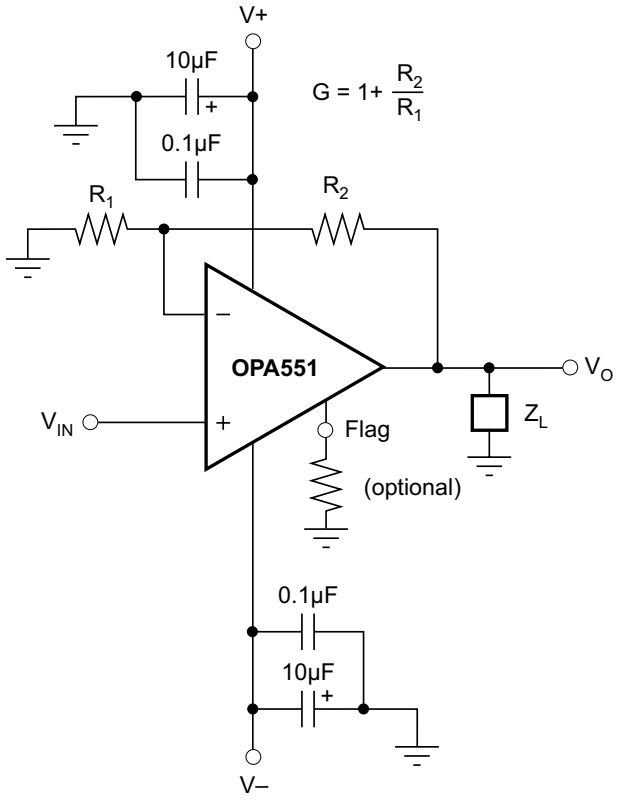


Figure 27. Basic Circuit Connections

8.2.1 Design Requirements

- Operate from power supplies between ±15 V to ±30 V
- Drive passive and reactive loads up to 1 A
- Drive large capacitive loads
- Operate up to 125°C

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitive Loads

The dynamic characteristics of the OPA55x have been optimized for commonly-encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load decreases the phase margin and may lead to gain peaking or oscillations. Figure 28 shows a circuit that preserves phase margin with a 10-nF capacitive load. Figure 33 shows the small-signal step response for the circuit in Figure 28. Consult SBOA015 for more information.

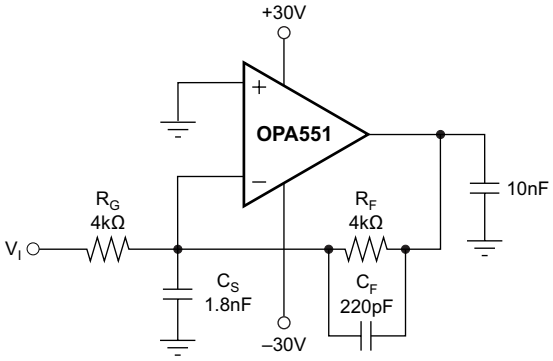
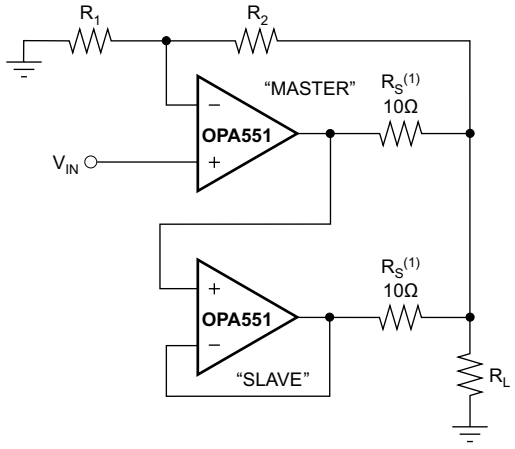


Figure 28. Driving Large Capacitive Loads

8.2.2.2 Increasing Output Current

In those applications where the 200 mA of output current is not sufficient to drive the desired load, output current can increase by connecting two or more OPA551s or OPA552s in parallel, as shown in Figure 29. Amplifier A1 is the *master* amplifier and may be configured in virtually an operational amplifier circuit. Amplifier A2, the *slave*, is configured as a unity-gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 30 is capable of supplying output currents up to 1 A. Alternatively, consider the OPA547, OPA548, and OPA549 series power operational amplifiers for high output current drive, along with programmable current limit and output disable capability.



NOTE: (1) R_S resistors minimize the circulating current that can flow between the two devices due to V_{OS} errors.

Figure 29. Parallel Amplifiers Increase Output Current Capability

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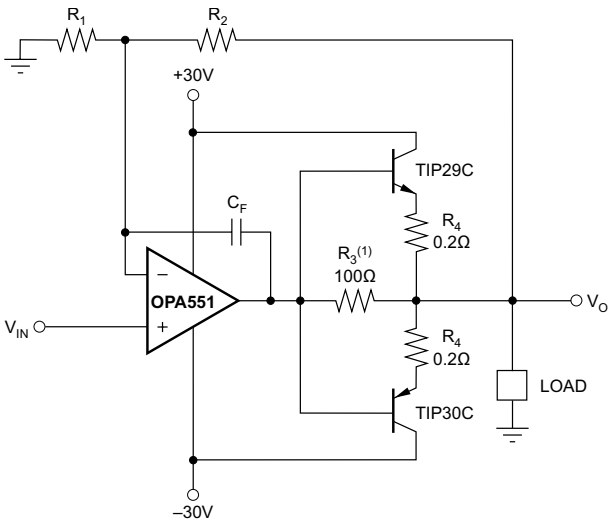
Typical Application (continued)



NOTE: (1) R_3 provides current limit and allows the amplifier to drive the load when the output is between 0.7V and –0.7V.

Figure 30. External Output Transistors Boost Output Current Up to 1 A

8.2.2.3 Using the OPA552 in Low Gains

The OPA552 family is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of the high slew rate in lower gains using an external compensation technique in an inverting configuration. This technique maintains low-noise characteristics of the OPA552 architecture at low frequencies. Depending on the application, a small increase in high-frequency noise may result. This technique shapes the loop gain for good stability while giving an easily-controlled, second-order, lowpass frequency response.

Considering only the noise gain (noninverting signal gain) for the circuit of Figure 31, the low-frequency noise gain (NG_1) is set by the resistor ratios, while the high-frequency noise gain (NG_2) is set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S / C_F$, is set to a value greater than the recommended minimum stable gain for the operational amplifier and the noise gain pole, set by $1 / R_F C_F$, is placed correctly, a very well-controlled, second-order, lowpass frequency response is the result.

To choose the values for both C_S and C_F, two parameters and only three equations must be solved. First, the target for the high-frequency noise gain (NG_2) must be greater than the minimum stable gain for the OPA552. In the circuit shown in Figure 31, a target NG_2 of 10 is used. Second, the signal gain of –1 shown in Figure 31 sets the low frequency noise gain to $NG_1 = 1 + R_F / R_G$ (= 2 in this example). Using these two gains, knowing the gain bandwidth product (GBP) for the OPA552 (12 MHz), and targeting a maximally flat, second-order, lowpass Butterworth frequency response (Q = 0.707), the key frequency in the compensation can be found.

For the values shown in Figure 31, the f_{-3dB} is approximately 956 kHz. This frequency is less than that predicted by simply dividing the GBP by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance as a result of increased loop gain at frequencies below $NG_1 \times Z_0$. The capacitor values shown in Figure 31 are calculated for $NG_1 = 2$ and $NG_2 = 10$ with no adjustment for parasitics.

Optimize the actual circuit values by checking the small-signal step response with actual load conditions. Figure 32 shows the small-signal step response of this OPA552, G = –1 circuit with a 500-pF load. It is well-behaved with no tendency to oscillate. If C_S and C_F are removed, the circuit becomes unstable.

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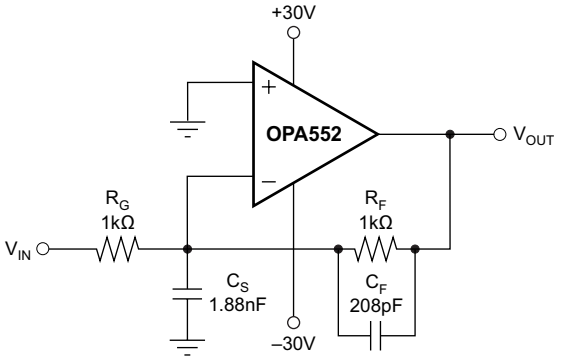
Typical Application (continued)



$NG_1 = 1 + R_F/R_G = 2$
$NG_2 = 1 + C_S/C_F = 10$

Figure 31. Compensation of the OPA552 for G = 1

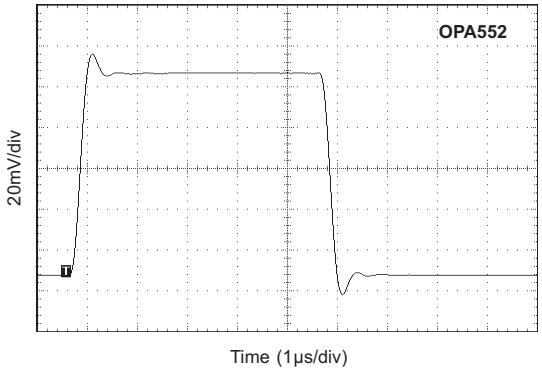


Figure 32. Small-Signal Step Response for Figure 31

8.2.2.4 Offset Voltage Error Calculation

The offset voltage (V_{OS}) of the OPA51 and OPA552 is specified with a ±30-V power supply and the common-mode voltage centered between the supplies (V_S / 2 = 0 V). Additional specifications for power-supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case excepted offset under the conditions of a given application.

Power-supply rejection ratio (PSRR) is specified in µV/V. For the OPA55x, worst-case PSRR is 30 µV/V, which means for each volt of change in total power-supply voltage, the offset may shift by up to 30 µV/V. Common-mode rejection ratio (CMRR) is specified in dB, which can be converted to µV/V using Equation 1:

$$\text{CMRR in (V/V)} = 10^{[(\text{CMRR in dB})/-20]} \quad (1)$$

For the OPA55x, the worst-case CMRR at ±30-mV supply over the full common-mode range is 96 dB, or approximately 15.8 µV/V. This result means that for every volt of change in common-mode, the offset may shift up to 15.8 µV. These numbers can be used to calculate excursions from the specified offset voltage under different applications conditions. For example, a common application might configure the amplifier with a –48-V single supply with –6-V common-mode. This configuration represents a 12-V variation in power supply: ±30 V or 60 V in the offset specification versus 48 V in the application. In addition, this configuration has an 18-V variation in common-mode voltage: V_S / 2 = –24 V is the specification for these power supplies, but the common-mode voltage is –6 V in the application.

Calculation of the worst-case expected offset for this example is calculated by Equation 2 and Equation 3.

$$\text{Worst-case } V_{OS} = \text{maximum specified } V_{OS} + (\text{power-supply variation} \times \text{PSRR}) + (\text{common-mode variation} \times \text{CMRR}) \quad (2)$$

$$V_{OSwc} = 5\text{ mV} + (12\text{ V} \times 30\text{ µV/V}) + (18\text{ V} \times 15.8\text{ µV/V}) = \pm 5.64\text{ mV} \quad (3)$$

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Typical Application (continued)

8.2.3 Application Curve

Figure 33 shows the small-signal step response for the circuit in Figure 28. Consult AB-028 for more information.

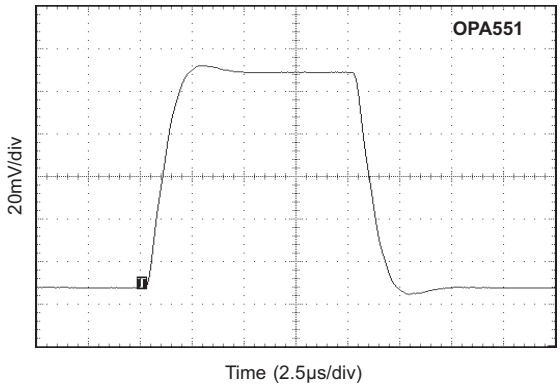

Figure 33. Small-Signal Step Response for Driving Large Capacitive Loads

9 Power Supply Recommendations

9.1 Power Supplies

The OPA55x may be operated from power supplies of ±4 V to ±30 V, or a total of 60 V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the *Typical Characteristics*.

For applications that do not require symmetrical output voltage swing, power-supply voltages do not need to be equal. The OPA55x can operate with as little as 8 V between the supplies or with up to 60 V between the supplies. For example, the positive supply could be set to 50 V with the negative supply at –10 V, or vice-versa.

The SOIC-8 package outline shows three negative supply (V–) pins. These pins are internally connected for improved thermal performance.

NOTE

Pin 4 must be used as the primary current carrier for the negative supply. It is recommended that pins 1 and 5 are not directly connected to V–. Instead, connect pins 1 and 5 to a thermal mass. DO NOT lay out the printed-circuit-board (PCB) to use pins 1 and 5 as feedthroughs to the negative supply. Such a configuration results in a performance reduction.

The tab of the DDPAK/TO-263 package is electrically connected to the negative supply (V–). However, this connection must not be used to carry current. For best thermal performance, solder the tab directly to the PCB copper area (see the *Heat Sinking* section).

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10 Layout

10.1 Layout Guidelines

The circuit board must have as much ground plane area as possible. Power supply and output traces must be sized to handle the required current. Keep input and output terminals separated as much as possible.

10.2 Layout Example

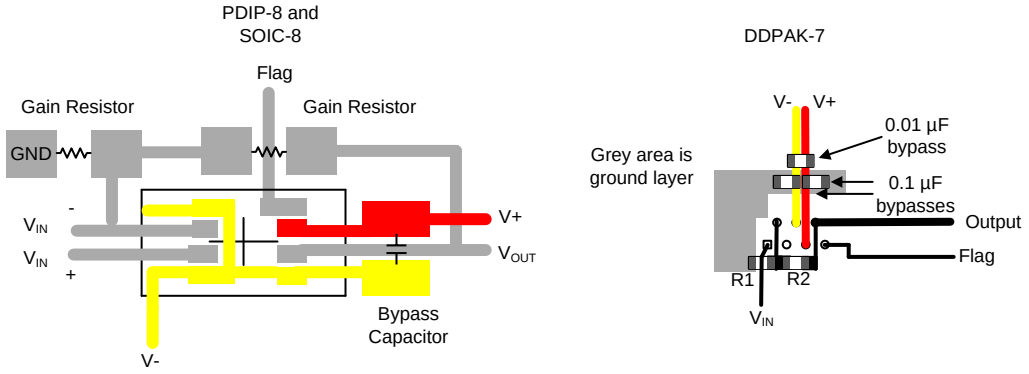

Figure 34. Layout Example (OPA551)

10.3 Power Dissipation

Internal power dissipation of these operational amplifiers can be quite large. Many of the specifications for the OPA55x are for a specified junction temperature. If the device is not subjected to internal self-heating, the junction temperature is the same as the ambient. However, in practical applications, the device self-heats and the junction temperature becomes significantly higher than ambient. After junction temperature has been established, performance parameters that vary with junction temperature can be determined from the performance curves. The following calculation can be performed to establish junction temperature as a function of ambient temperature and the conditions of the application.

Consider the OPA551 in a circuit configuration where the load is 600 Ω and the output voltage is 15 V. The supplies are at ±30 V and the ambient temperature (T_A) is 40°C. The θ_{JA} for the 8-pin PDIP package is 100°C/W.

First, the internal heating of the operational amplifier is in Equation 4:

$$P_{D(internal)} = I_Q \times V_S = 7.2\ mA \times 60\ V = 432\ mW \quad (4)$$

The output current (I_O) can be calculated in Equation 5:

$$I_O = V_{OUT}/R_L = 15\ V/600\ \Omega = 25\ mA \quad (5)$$

The power being dissipated (P_D) in the output transistor of the amplifier can be calculated in Equation 6 and Equation 7:

$$P_{D(output\ stage)} = I_O \times (V_S — V_O) = 25\ mA \times (30 – 15) = 375\ mW \quad (6)$$

$$P_{D(total)} = P_{D(internal)} + P_{D(output\ stage)} = 432\ mW + 375\ mW = 807\ mW \quad (7)$$

The resulting junction temperature can be calculated in Equation 8 and Equation 9:

$$T_J = T_A + P_D\ \theta_{JA} \quad (8)$$

$$T_J = 40°C + 807\ mW \times 100°C/W = 120.7°C$$

where

- T_J = junction temperature (°C)
- T_A = ambient temperature (°C)
- θ_{JA} = junction-to-air thermal resistance (°C/W) (9)

For the DDPAK/TO-263 package, the θ_{JA} is 65°C/W with no heat sinking, resulting in a junction temperature of 92.5°C.

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Power Dissipation (continued)

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection must trigger more than 35°C above the maximum expected ambient condition of a given application. This limit ensures a maximum junction temperature of 125°C at the maximum expected ambient condition.

If the OPA551 or OPA552 is to be used in an application requiring more than 0.5-W continuous power dissipation, TI recommends that the DDPAK/TO-263 package option be used. The DDPAK/TO-263 has superior thermal dissipation characteristics and is more easily adapted to a heatsink.

Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation because a larger voltage can be impressed across the conducting output transistor. Consult SBOA022 for further information on how to calculate or measure power dissipation.

Power dissipation can be minimized by using the lowest possible supply voltage. For example, with a 200-mA load, the output swings to within 3.5 V of the power-supply rails. Set the power supplies to no more than 3.5 V above the maximum output voltage swing required by the application to minimize the power dissipation.

10.4 Safe Operating Area

The Safe Operating Area (SOA) curves Figure 35, Figure 36, and Figure 37 show the permissible range of voltage and current. These curves shown represent devices soldered to a circuit board with no heatsink. The safe output current decreases as the voltage across the output transistor (V_S – V_O) increases. For further insight on SOA, consult AB-039.

Output short circuits are a very demanding case for SOA. A short-circuit to ground forces the full power-supply voltage (V+ or V–) across the conducting transistor and produces a typical output current of 380 mA. With ±30-V power supplies, this configuration creates an internal dissipation of 11.4 W. This dissipation far exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, use the DDPAK/TO-263 package with a heatsink.

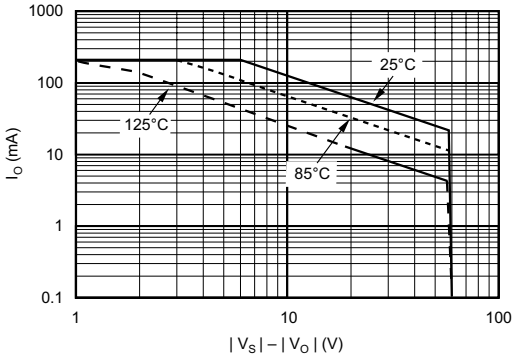

Figure 35. PDIP-8 Safe Operating Area

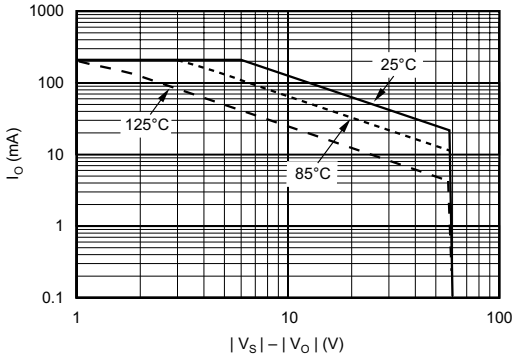

Figure 36. SOIC-8 Safe Operating Area

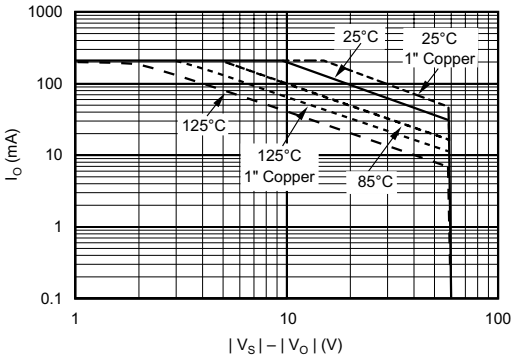

Figure 37. DDPAK-7/TO-263 Safe Operating Area

10.5 Heat Sinking

Power dissipated in the OPA551 or OPA552 causes the junction temperature to rise. For reliable operation, limit the junction temperature to 125°C. Many applications require a heatsink to assure that the maximum operating junction temperature is not exceeded. The heatsink required depends on the power dissipated and on ambient conditions.

For heatsinking purposes, the tab of the DDPAK/TO-263 is typically soldered directly to the PCB copper area. Increasing the copper area improves heat dissipation. Figure 38 shows typical thermal resistance from junction-to-ambient as a function of copper area.

Depending on conditions, additional heatsinking may be required. Aavid Thermal Products Inc. manufactures surface-mountable heatsinks designed specifically for use with DDPAK/TO-263 packages. Further information is available on the Aavid web site, www.aavid.com.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection must trigger more than 25°C above the maximum expected ambient condition of your application. This level produces a junction temperature of 125°C at the maximum expected ambient condition.

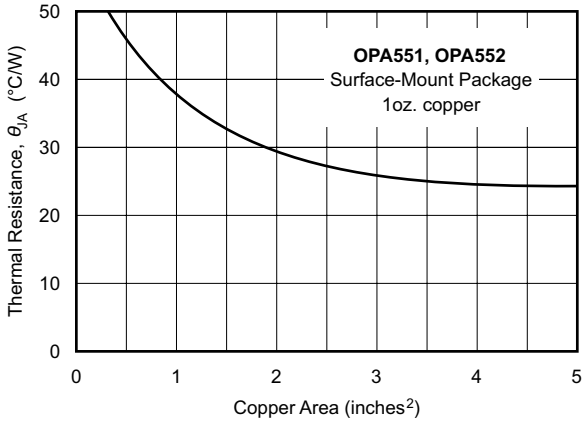

Figure 38. Thermal Resistance vs Circuit Board Copper Area

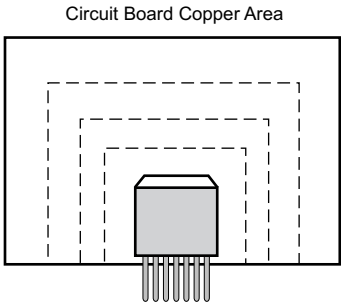

Figure 39. OPA551, OPA552 Surface-Mount Package Circuit Board Copper Area

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA551	Click here	Click here	Click here	Click here	Click here
OPA552	Click here	Click here	Click here	Click here	Click here

11.2.2 Related Documentation

For related documentation, please see the following:

- *Heat Sinking — TO-3 Thermal Mode* (SBOA021)
- *Application bulletin AB-028: Feedback Plots Define Op Amp AC Performance* (SBOA015)
- *Application bulletin AB-039: Power Amplifier Stress and Power Handling Limitations* (SBOA022)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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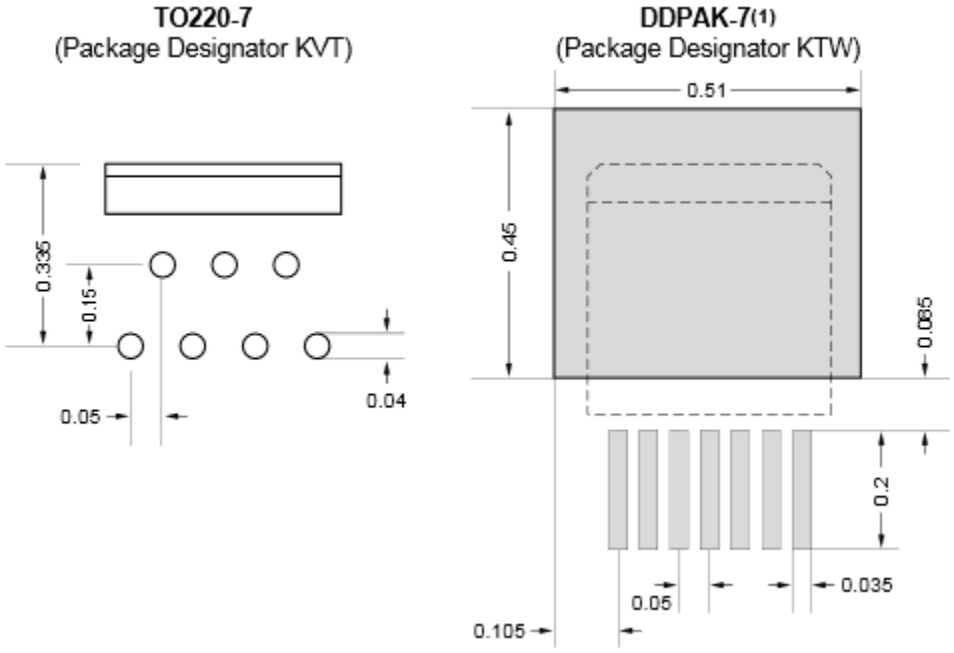
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



(1) For improved thermal performance, increase footprint area.

(2) Mean dimensions in inches. Refer to the mechanical drawings or www.ti.com for tolerances and detailed package drawings.

Figure 40. TO-220 and DDPAK Solder Footprints

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA551FA/500	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA551FA
OPA551FA/500.A	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA551FA
OPA551FA/500G3	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA551FA
OPA551FAKTWT	Active	Production	DDPAK/TO-263 (KTW) | 7	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA551FA
OPA551FAKTWT.A	Active	Production	DDPAK/TO-263 (KTW) | 7	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA551FA
OPA551PA	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	OPA551PA
OPA551PA.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	OPA551PA
OPA551UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 551UA
OPA551UA.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 551UA
OPA551UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 551UA
OPA551UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 551UA
OPA552FA/500	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA552FA
OPA552FA/500.A	Active	Production	DDPAK/TO-263 (KTW) | 7	500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA552FA
OPA552FAKTWT	Active	Production	DDPAK/TO-263 (KTW) | 7	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-	OPA552FA
OPA552FAKTWT.A	Active	Production	DDPAK/TO-263 (KTW) | 7	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	OPA552FA
OPA552UA	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-	OPA 552UA
OPA552UA.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 552UA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA552UA/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-	OPA 552UA
OPA552UA/2K5.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 552UA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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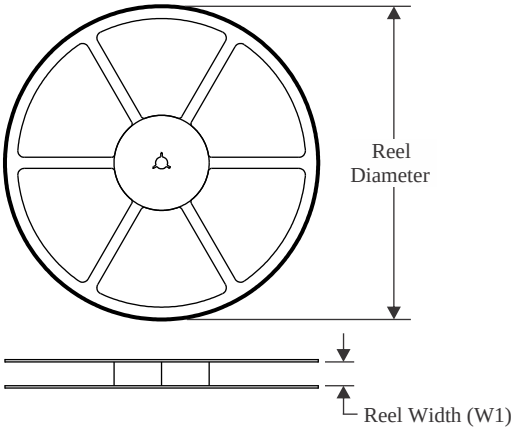
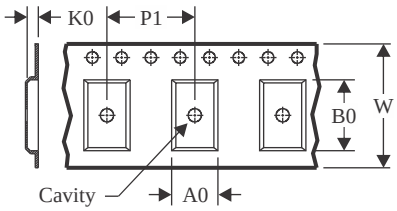
TAPE AND REEL INFORMATION

REEL DIMENSIONS

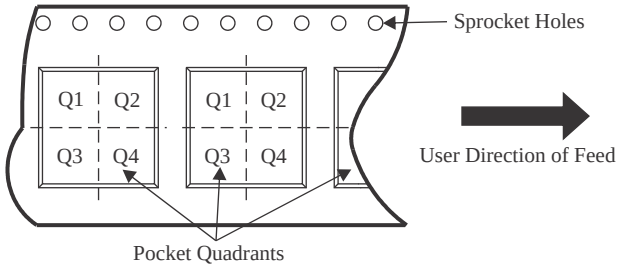


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

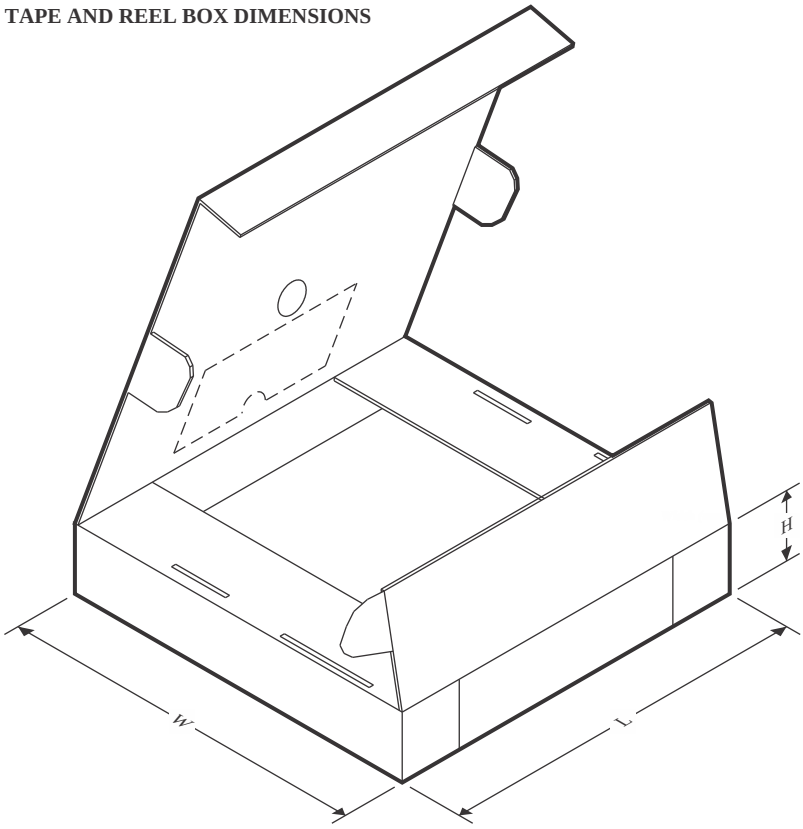
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA551FA/500	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA551FAKTWT	DDPAK/ TO-263	KTW	7	250	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA551UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA552FA/500	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA552FAKTWT	DDPAK/ TO-263	KTW	7	250	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
OPA552UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

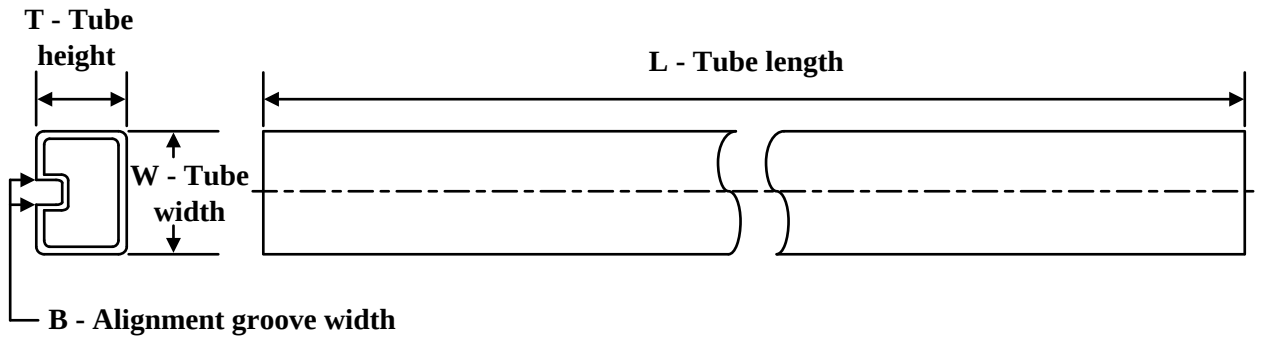
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA551FA/500	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0
OPA551FAKTWT	DDPAK/TO-263	KTW	7	250	356.0	356.0	45.0
OPA551UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA552FA/500	DDPAK/TO-263	KTW	7	500	356.0	356.0	45.0
OPA552FAKTWT	DDPAK/TO-263	KTW	7	250	356.0	356.0	45.0
OPA552UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0

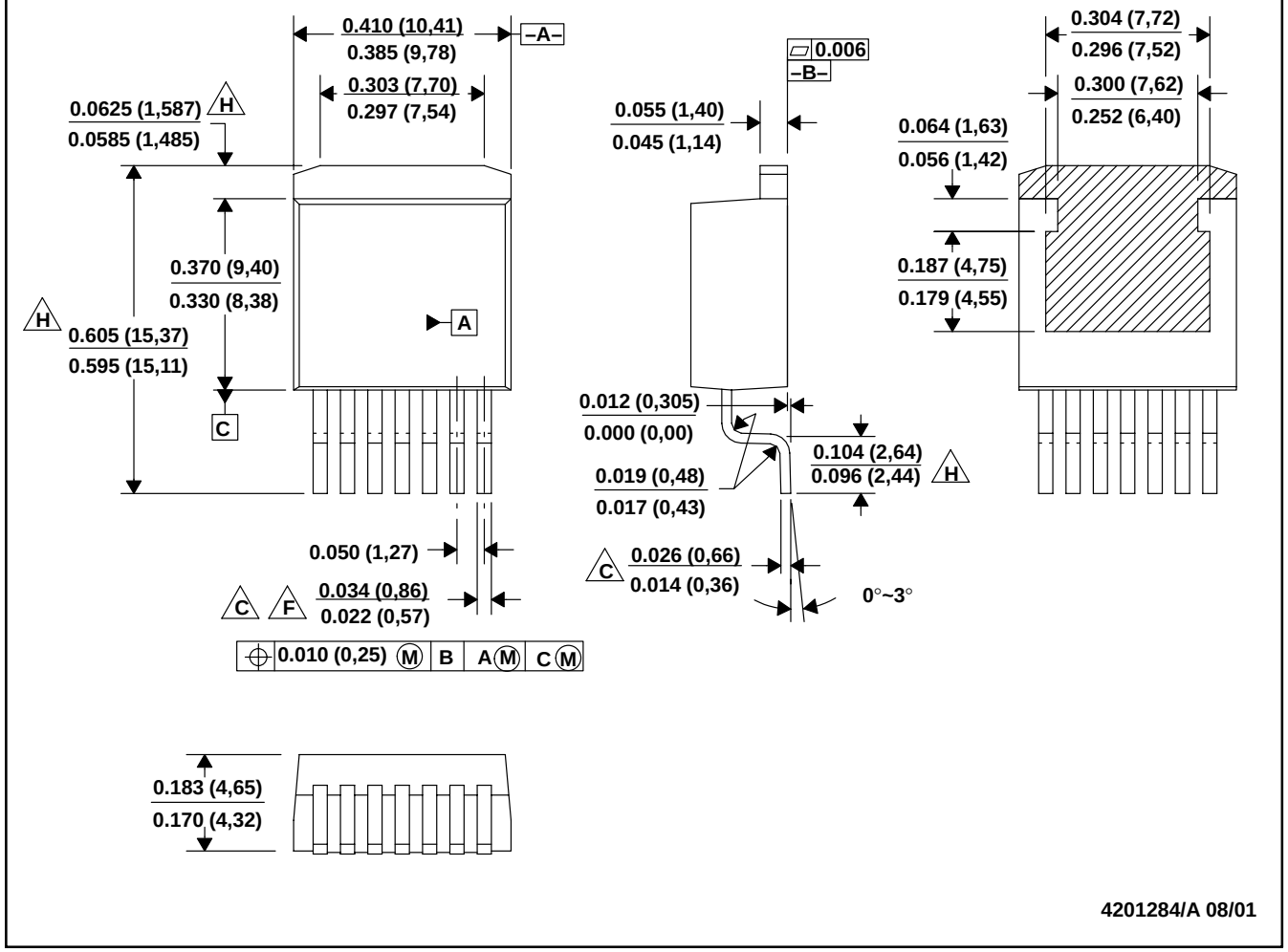
TUBE



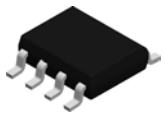
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA551PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA551PA.A	P	PDIP	8	50	506	13.97	11230	4.32
OPA551UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA551UA.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA552UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA552UA.A	D	SOIC	8	75	506.6	8	3940	4.32

KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

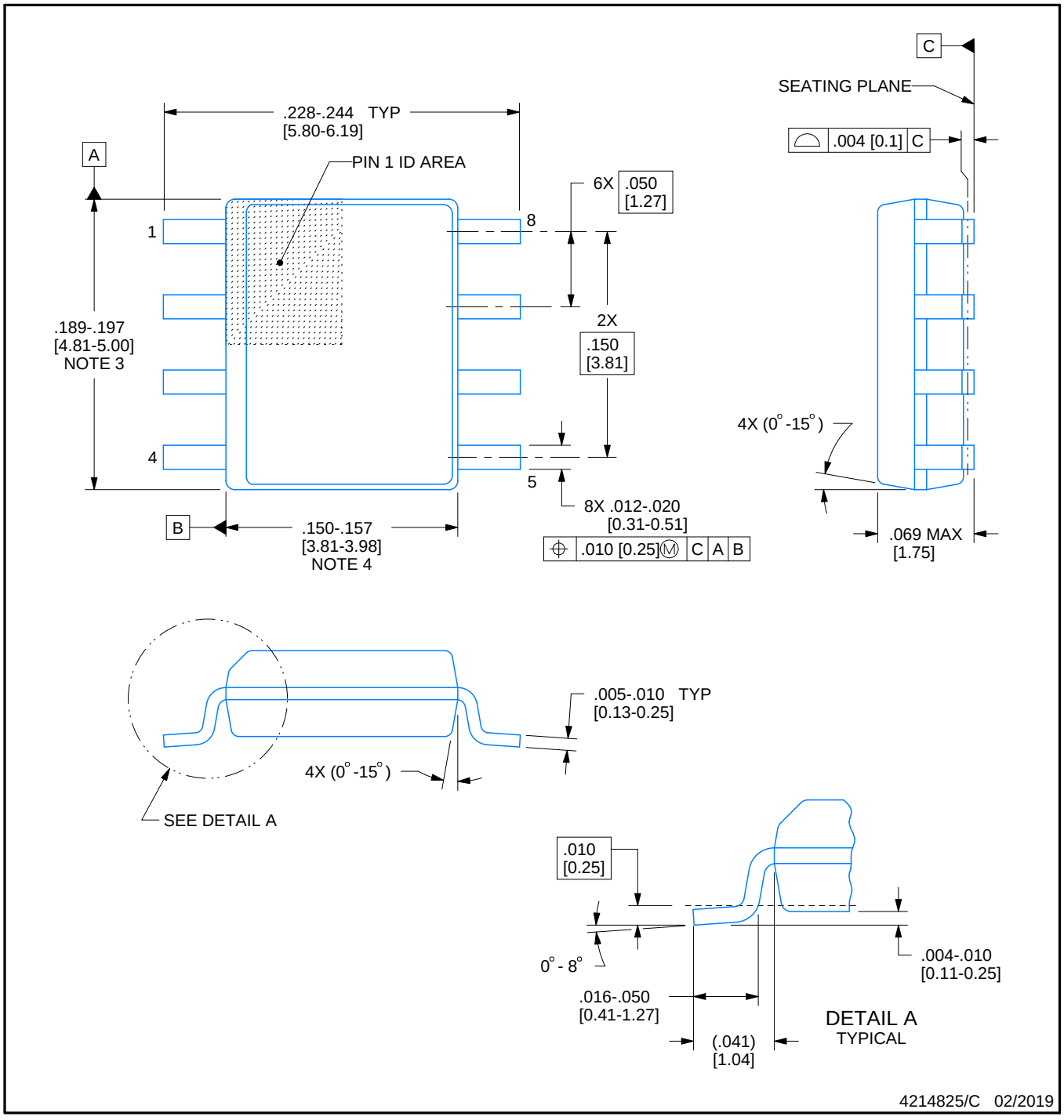


PACKAGE OUTLINE

D0008A

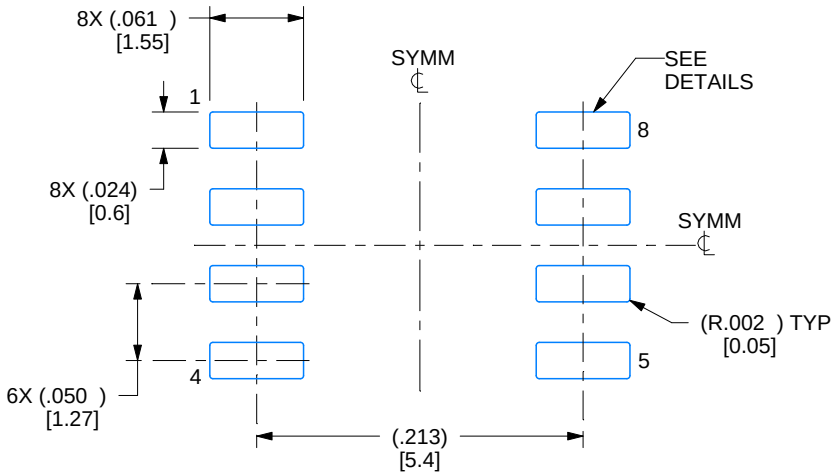
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

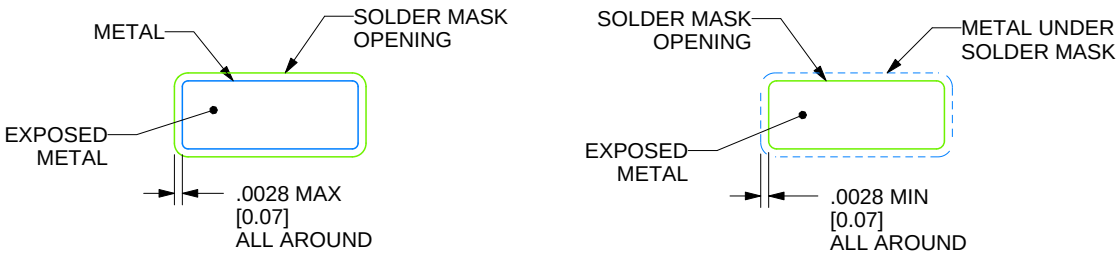


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

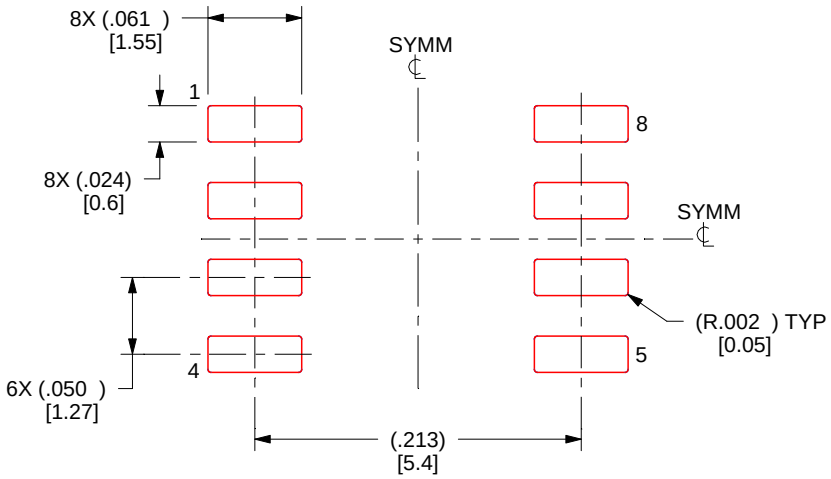
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



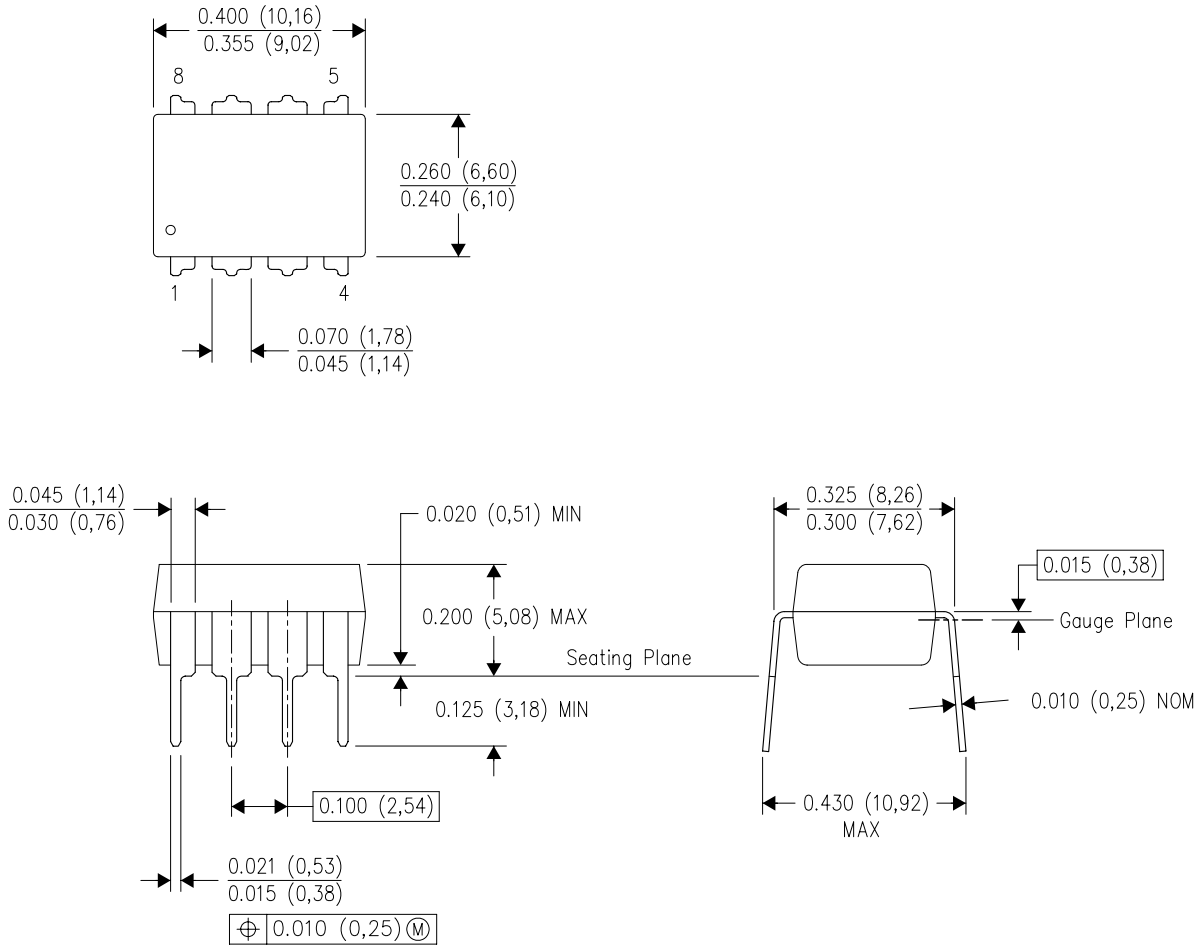
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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