OPAx992-Q1 汽车级 40V 轨到轨输入或输出、低失调电压、低噪声运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C 至 +125°C，T_A
  - 器件 HBM ESD 分类等级 2A
  - 器件 CDM ESD 分类等级 C6
- 低失调电压：±210μV
- 低失调电压漂移：±0.25μV/°C
- 低噪声：1kHz 时为 7nV/√Hz，4.4nV/√Hz 宽带
- 高共模抑制：115dB
- 低偏置电流：±10pA
- 轨到轨输入和输出
- 支持多路复用器/比较器输入
  - 放大器以最高达到电源轨的差分输入工作
  - 放大器可用于开环中，也可用作比较器
- 高带宽：10.6MHz GBW，单位增益稳定
- 高压摆率：32V/μs
- 低静态电流：每个放大器 2.4mA
- 宽电源电压：±1.35V 至 ±20V，2.7V 至 40V
- 强大的 EMIRR 性能

2 应用

- 汽车音响主机
- 汽车外部放大器
- 紧急呼叫 (eCall)
- 远程信息处理控制单元 (TCU)
- 牵引逆变器
- HEV/EV 车载无线充电器 (OBC)
- HEV/EV 直流/直流转换器
- 高侧和低侧电流检测

3 说明

OPAx992-Q1 系列（OPA992-Q1、OPA2992-Q1 和 OPA4992-Q1）是高电压 (40V) 通用运算放大器系列。这些器件具有出色的直流精度和交流性能，包括轨到轨输入或输出、低失调电压（典型值为 ±210μV）、低温漂（典型值为 ±0.25μV/°C）和低噪声（1kHz 时为 7nV/√Hz，10kHz 时为 4.4nV/√Hz）。

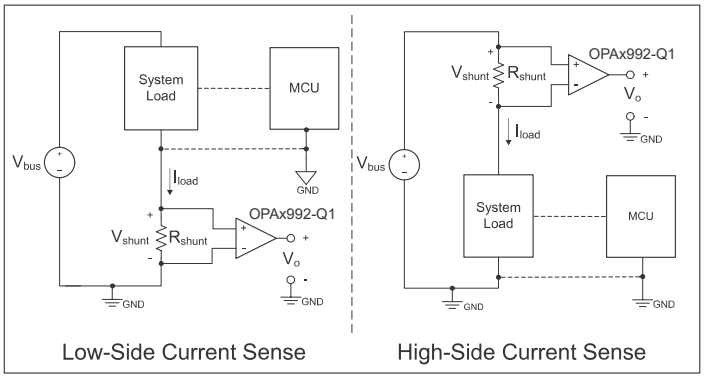
OPAx992-Q1 具有诸多特性，例如差分和共模输入电压范围（高达电源轨电压）、高短路电流 (±65mA) 和高压摆率 (32V/μs)，是一款灵活可靠的高性能运算放大器，适用于各种高压汽车应用。

OPAx992-Q1 系列运算放大器采用标准封装（如 SOIC、TSSOP、VSSOP、SOT-23 和 SC70），其额定工作温度范围为 –40°C 至 125°C。

封装信息

器件型号(1)	封装	封装尺寸(2)
OPA992-Q1	DCK（SC70，5）	2mm × 2.1mm
	DBV（SOT-23，5）	2.9mm × 2.8mm
OPA2992-Q1	DGK（VSSOP，8）	3mm × 4.9mm
	PW（TSSOP，8）	3mm × 6.4mm
	D（SOIC，8）	4.9mm × 6mm
OPA4992-Q1	PW（TSSOP，14）	5mm × 6.4mm
	D（SOIC，14）	8.65mm × 6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



在电流检测应用中的 OPAx992-Q1

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Pin Configuration and Functions 3
5 Specifications 6
5.1 Absolute Maximum Ratings 6
5.2 ESD Ratings 6
5.3 Recommended Operating Conditions 6
5.4 Thermal Information for Single Channel 7
5.5 Thermal Information for Dual Channel 7
5.6 Thermal Information for Quad Channel 7
5.7 Electrical Characteristics 8
5.8 Typical Characteristics 10
6 Detailed Description 18
6.1 Overview 18
6.2 Functional Block Diagram 18
6.3 Feature Description 19
6.4 Device Functional Modes 27
7 Application and Implementation 28
7.1 Application Information 28
7.2 Typical Applications 28
7.3 Power Supply Recommendations 29
7.4 Layout 30
8 Device and Documentation Support 32
8.1 Device Support 32
8.2 Documentation Support 32
8.3 接收文档更新通知 32
8.4 支持资源 32
8.5 Trademarks 32
8.6 静电放电警告 32
8.7 术语表 32
9 Revision History 33
10 Mechanical, Packaging, and Orderable Information 33

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

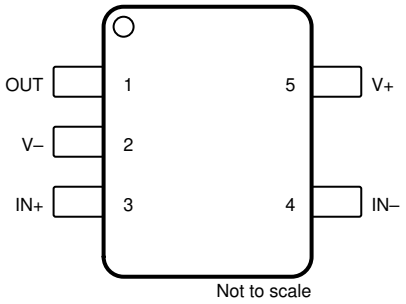


图 4-1. OPA992-Q1 DBV Package, 5-Pin SOT-23 (Top View)

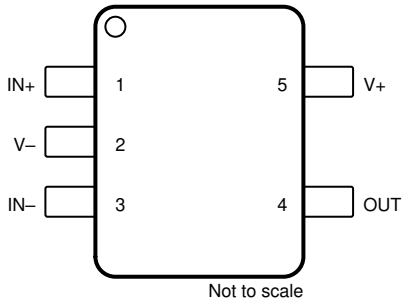


图 4-2. OPA992-Q1 DCK Package, 5-Pin SC70 (Top View)

表 4-1. Pin Functions: OPA992-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70		
IN+	3	1	I	Noninverting input
IN –	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V –	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

Copyright © 2024 Texas Instruments Incorporated

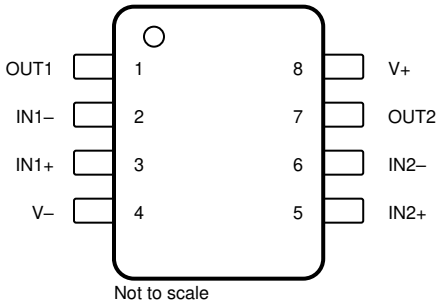


图 4-3. OPA2992-Q1 D, PW, and DGK Package, 8-Pin SOIC, TSSOP, and VSSOP (Top View)

表 4-2. Pin Functions: OPA2992-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V –	4	—	Negative (lowest) power supply

(1) I = input, O = output

Copyright © 2024 Texas Instruments Incorporated

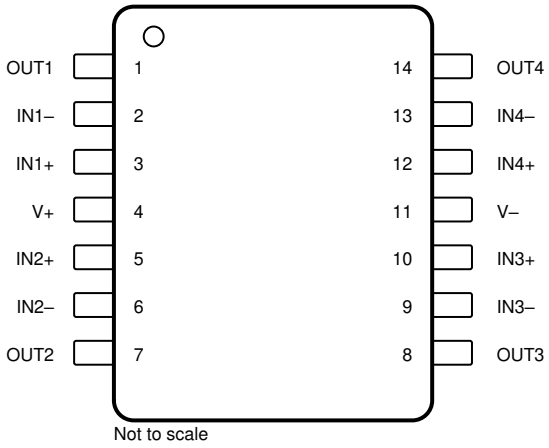


图 4-4. OPA4992-Q1 D and PW Package, 14-Pin SOIC and TSSOP (Top View)

表 4-3. Pin Functions: OPA4992-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1 –	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2 –	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 –	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 –	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V –	11	—	Negative (lowest) power supply

(1) I = input, O = output

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
OPA992-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1500	
OPA2992-Q1 and OPA4992-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	40	V
V_I	Common mode voltage range	(V–)	(V+)	V
T_A	Specified temperature	–40	125	°C

Copyright © 2024 Texas Instruments Incorporated

5.4 Thermal Information for Single Channel

THERMAL METRIC(1)		OPA992-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	202.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.8	111.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	51.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.6	25.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	51.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		OPA2992-Q1			Unit
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.8	159.1	173.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.0	67.9	65.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.3	98.1	95.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.8	9.1	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.5	96.7	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		OPA4992-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	63.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.0	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

Copyright © 2024 Texas Instruments Incorporated

5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.21	±1.03	mV
			T_A = –40°C to 125°C			±1.2	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±0.25		µV/℃
PSRR	Input offset voltage versus power supply	OPA992-Q1, OPA2992-Q1, V_{CM} = V–, V_S = 5V to 40V	T_A = –40°C to 125°C		±0.2	±1.3	µV/V
		OPA4992-Q1, V_{CM} = V–, V_S = 5V to 40V			±0.4	±1.8	
		OPA992-Q1, OPA2992-Q1, OPA4992-Q1, V_{CM} = V–, V_S = 2.7V to 40V[1]			±0.8	±7	
	DC channel separation				0.4		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			2.77		μV_{PP}
					0.49		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			7		nV/√Hz
		f = 10kHz			4.4		
i_N	Input current noise density	f = 1kHz			60		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 40V, V– < V_{CM} < (V+) – 2V (PMOS pair)	T_A = –40°C to 125°C	100	115		dB
		V_S = 5V, V– < V_{CM} < (V+) – 2V (PMOS pair)[1]		75	98		
		V_S = 2.7V, V– < V_{CM} < (V+) – 2V (PMOS pair)			90		
		V_S = 2.7 – 40V, (V+) – 1V < V_{CM} < V+ (NMOS pair)			79		
		(V+) – 2V < V_{CM} < (V+) – 1V		See *Offset Voltage vs CommonMode Voltage (Transition Region)*			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V		120	142		dB
		V_S = 40V, V_{CM} = V_S / 2, (V–) + 0.12V < V_O < (V+) – 0.12V	T_A = –40°C to 125°C		142		
		V_S = 5V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V[1]		104	125		
			T_A = –40°C to 125°C		125		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V[1]		90	105		
			T_A = –40°C to 125°C		105		

Copyright © 2024 Texas Instruments Incorporated

For V_S = (V+) – (V –) = 2.7V to 40V (±1.35V to ±20V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

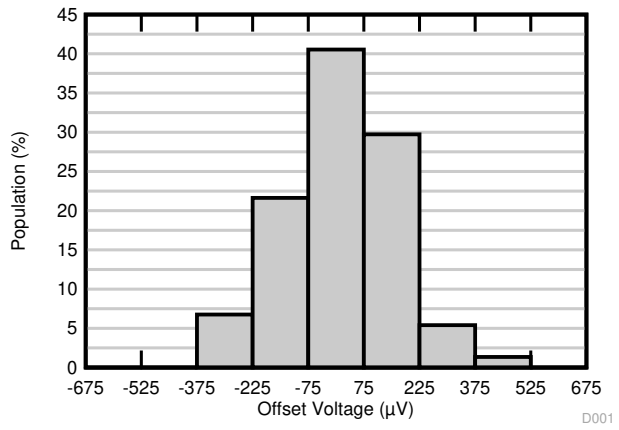
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				10.6		MHz
SR	Slew rate	V_S = 40V, G = +1, V_{STEP} = 10V, C_L = 20pF(3)			32		V/µs
t_S	Settling time	To 0.1%, V_S = 40V, V_{STEP} = 10V, G = +1, C_L = 20pF			0.65		µs
		To 0.1%, V_S = 40V, V_{STEP} = 2V, G = +1, C_L = 20pF			0.3		
		To 0.01%, V_S = 40V, V_{STEP} = 10V, G = +1, C_L = 20pF			0.86		
		To 0.01%, V_S = 40V, V_{STEP} = 2V, G = +1, C_L = 20pF			0.44		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			64		°
	Overload recovery time	V_{IN} × gain > V_S			170		ns
THD+N	Total harmonic distortion + noise	V_S = 40V, V_O = 3V_{RMS}, G = 1, f = 1kHz, R_L = 10kΩ			0.00005%		
					126		dB
		V_S = 10V, V_O = 3V_{RMS}, G = 1, f = 1kHz, R_L = 128Ω			0.0032%		
					90		dB
		V_S = 10V, V_O = 0.4V_{RMS}, G = 1, f = 1kHz, R_L = 32Ω			0.00032%		
					110		dB
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40V, R_L = no load		7		mV
			V_S = 40V, R_L = 10kΩ		48	60	
			V_S = 40V, R_L = 2kΩ		220	300	
			V_S = 2.7V, R_L = no load		0.5		
			V_S = 2.7V, R_L = 10kΩ		5	20	
			V_S = 2.7V, R_L = 2kΩ		20	50	
I_{SC}	Short-circuit current				±65(2)		mA
C_{LOAD}	Capacitive load drive				See *Phase Margin vs Capacitive Load*		pF
Z_O	Open-loop output impedance	I_O = 0A			See *Open-Loop Output Impedance vs Frequency*		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	OPA2992-Q1, OPA4992-Q1, I_O = 0A			2.4	2.8	mA
			T_A = –40°C to 125°C			2.84	
		OPA992, I_O = 0A			2.48	2.92	
			T_A = –40°C to 125°C			2.98	

(1) Specified by characterization only.
(2) At high supply voltage, placing the OPAx992 in a sudden short to mid-supply or ground will lead to rapid thermal shutdown. Output current greater than I_{SC} can be achieved if rapid thermal shutdown is avoided as per *Output Voltage Swing vs Output Current* .
(3) See *Slew Rate vs Input Step Voltage* for more information.

Copyright © 2024 Texas Instruments Incorporated

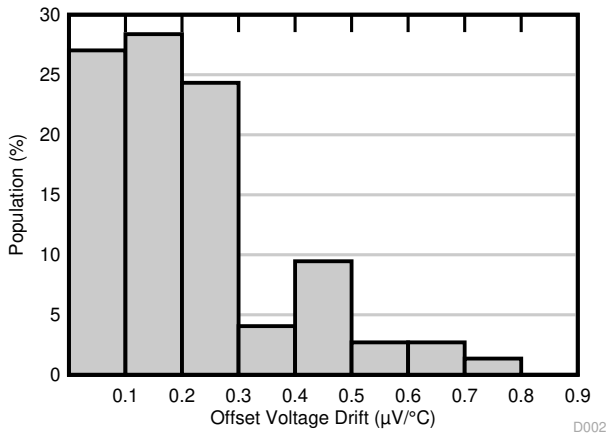
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



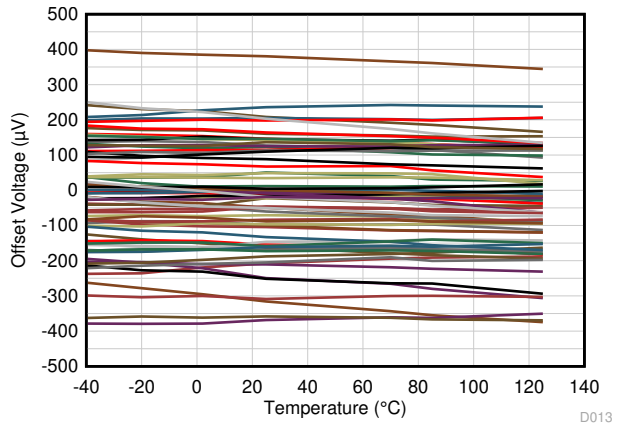
Distribution from 74 amplifiers, T_A = 25°C

图 5-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

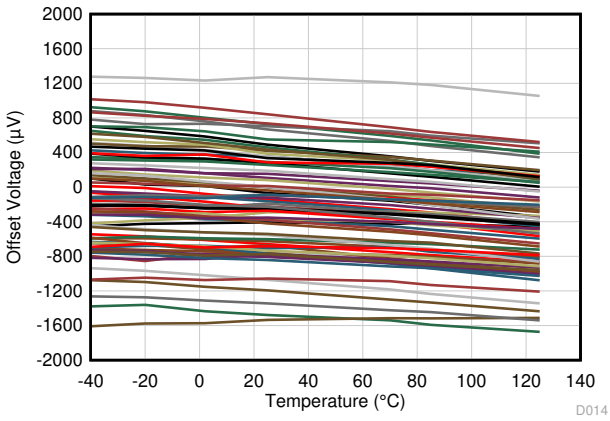
图 5-2. Offset Voltage Drift Distribution



V_{CM} = V –

Data from 74 amplifiers

图 5-3. Offset Voltage vs Temperature



V_{CM} = V+

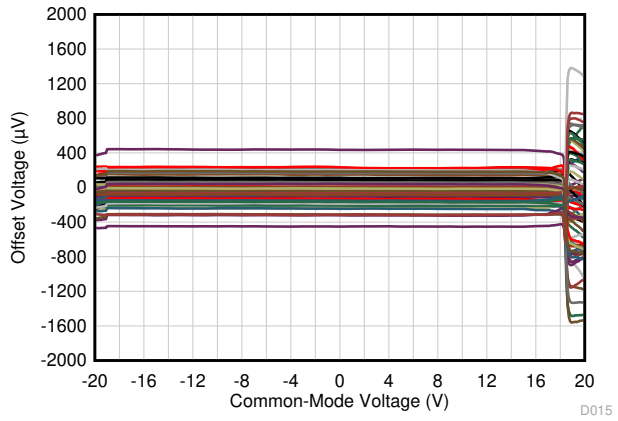
Data from 74 amplifiers

图 5-4. Offset Voltage vs Temperature

Copyright © 2024 Texas Instruments Incorporated

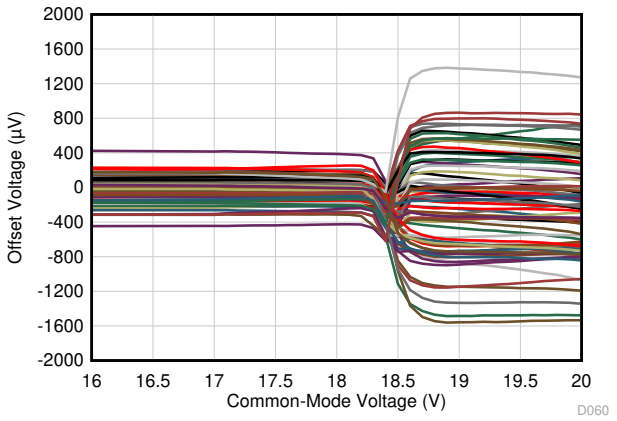
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



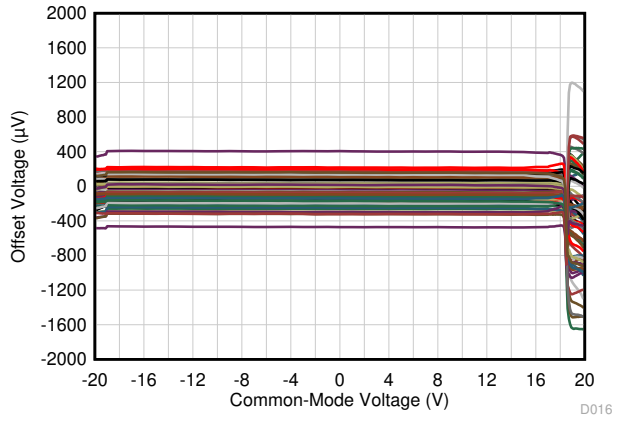
T_A = 25°C
Data from 74 amplifiers

图 5-5. Offset Voltage vs Common-Mode Voltage



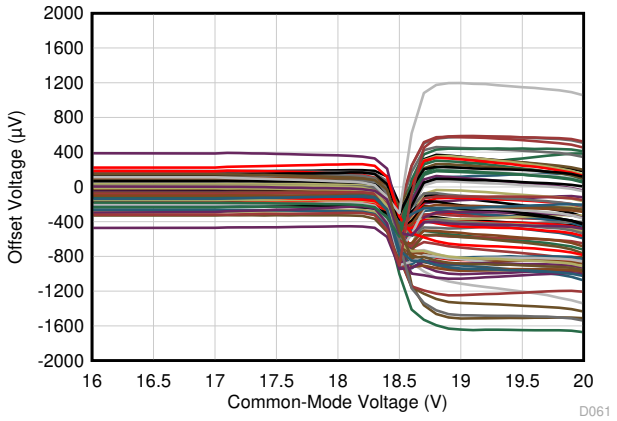
T_A = 25°C
Data from 74 amplifiers

图 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)



T_A = 125°C
Data from 74 amplifiers

图 5-7. Offset Voltage vs Common-Mode Voltage



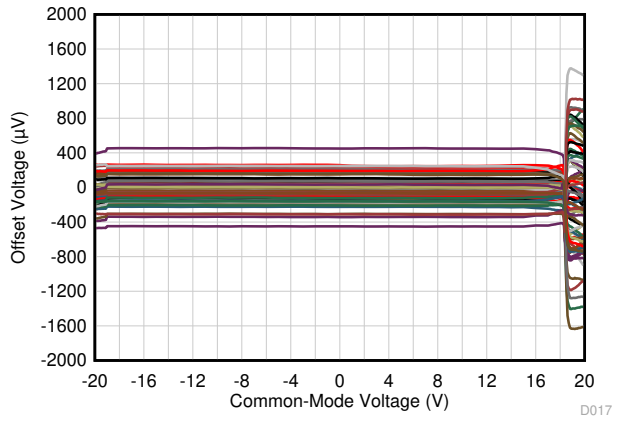
T_A = 125°C
Data from 74 amplifiers

图 5-8. Offset Voltage vs Common-Mode Voltage (Transition Region)

Copyright © 2024 Texas Instruments Incorporated

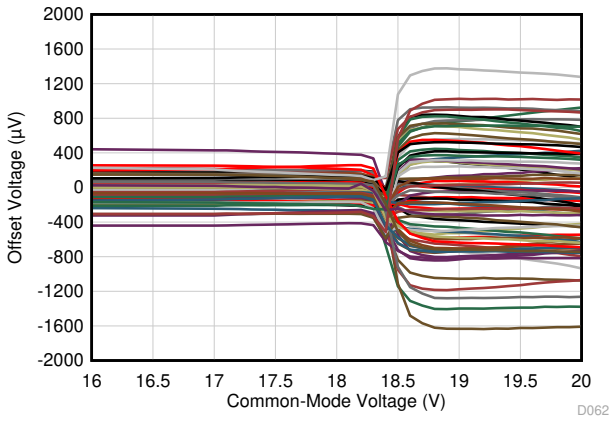
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



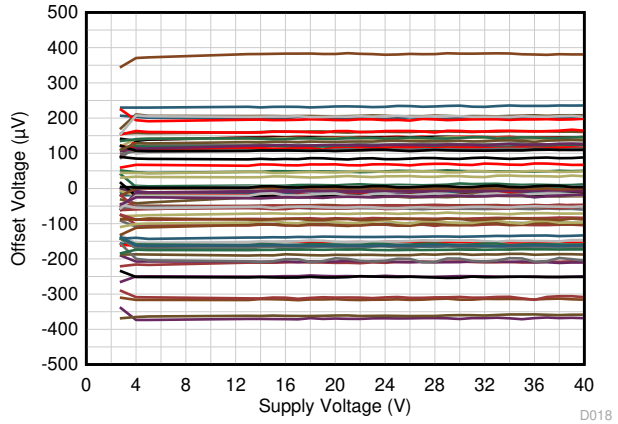
T_A = –40°C
Data from 74 amplifiers

图 5-9. Offset Voltage vs Common-Mode Voltage



T_A = –40°C
Data from 74 amplifiers

图 5-10. Offset Voltage vs Common-Mode Voltage (Transition Region)



V_{CM} = V –
Data from 74 amplifiers

图 5-11. Offset Voltage vs Power Supply

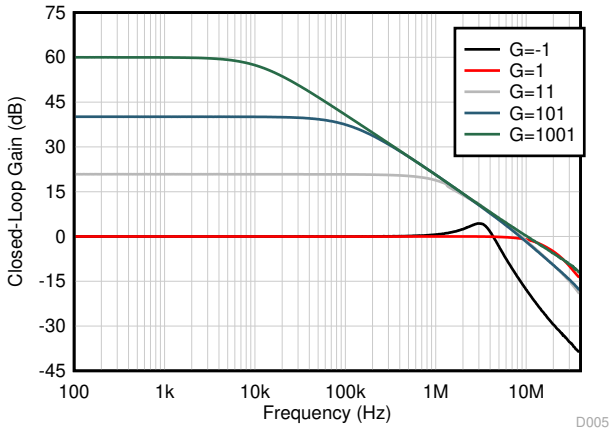


图 5-12. Closed-Loop Gain vs Frequency

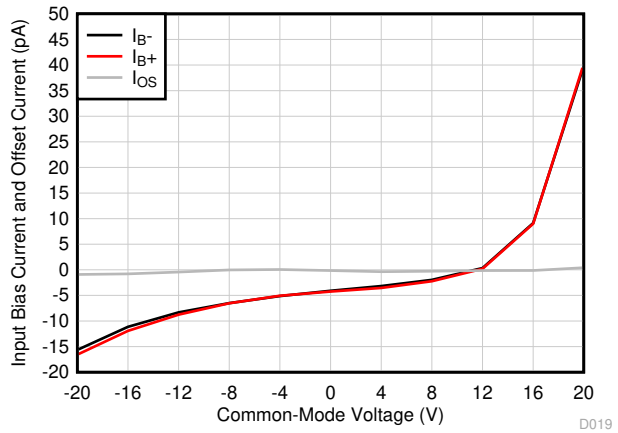


图 5-13. Input Bias Current and Offset Current vs Common-Mode Voltage

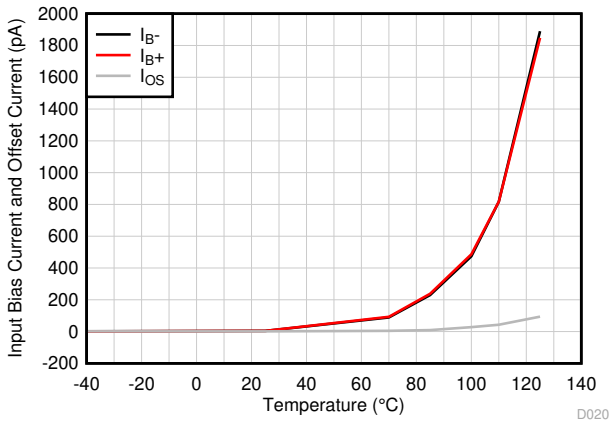


图 5-14. Input Bias Current and Offset Current vs Temperature

Copyright © 2024 Texas Instruments Incorporated

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

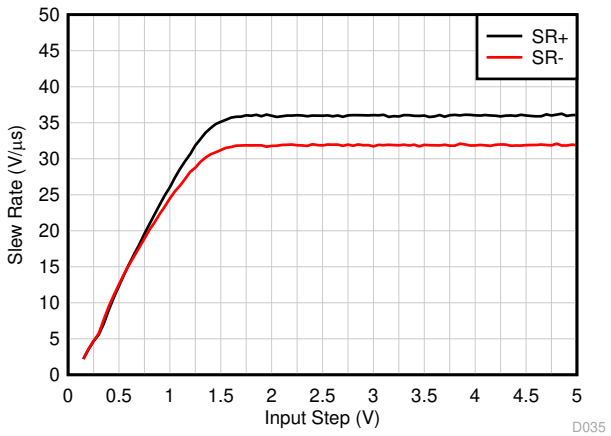
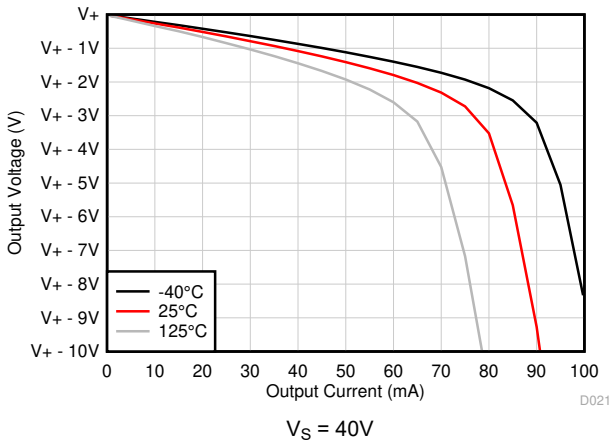
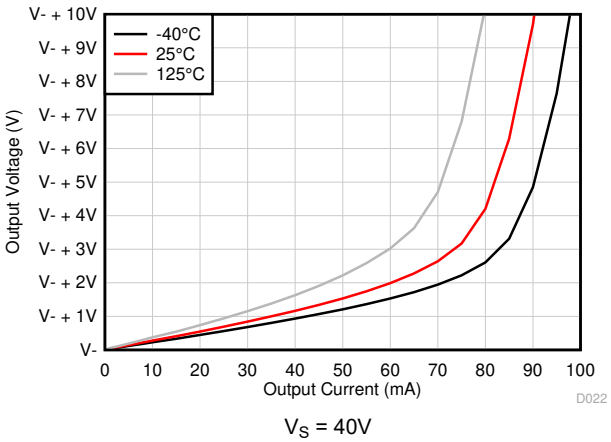


图 5-15. Slew Rate vs Input Step Voltage



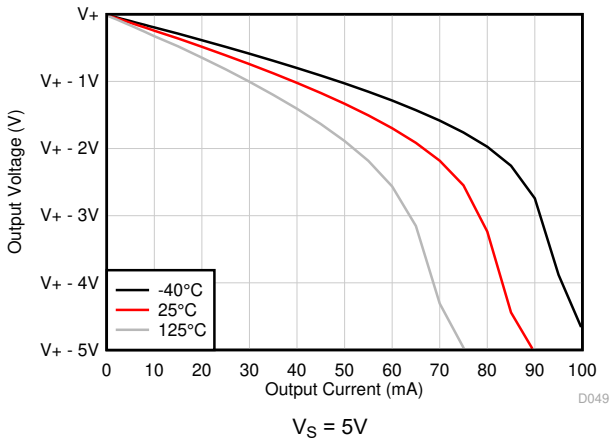
V_S = 40V

图 5-16. Output Voltage Swing vs Output Current (Sourcing)



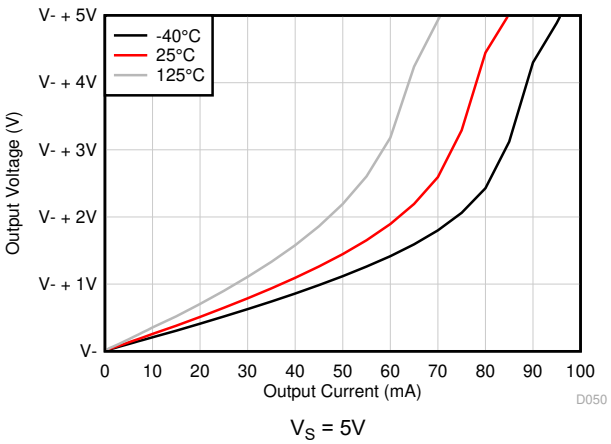
V_S = 40V

图 5-17. Output Voltage Swing vs Output Current (Sinking)



V_S = 5V

图 5-18. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5V

图 5-19. Output Voltage Swing vs Output Current (Sinking)

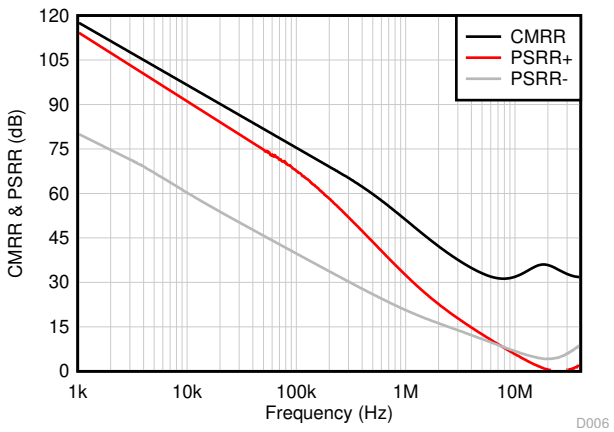
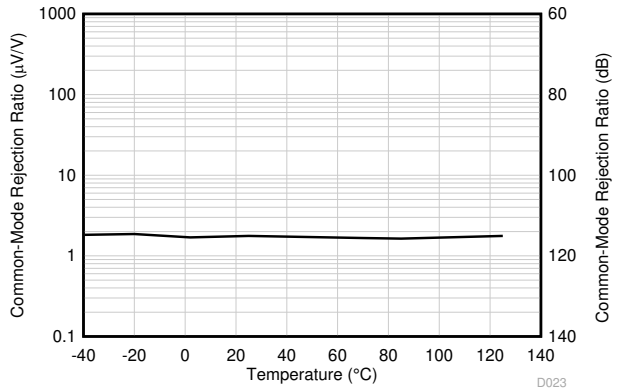


图 5-20. CMRR and PSRR vs Frequency

Copyright © 2024 Texas Instruments Incorporated

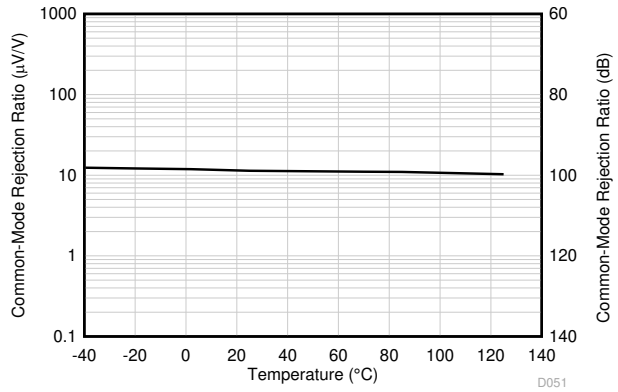
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



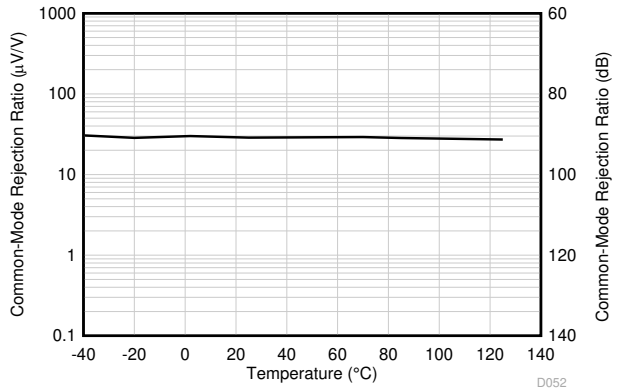
V_S = 40V

图 5-21. CMRR vs Temperature



V_S = 5V

图 5-22. CMRR vs Temperature



V_S = 2.7V

图 5-23. CMRR vs Temperature

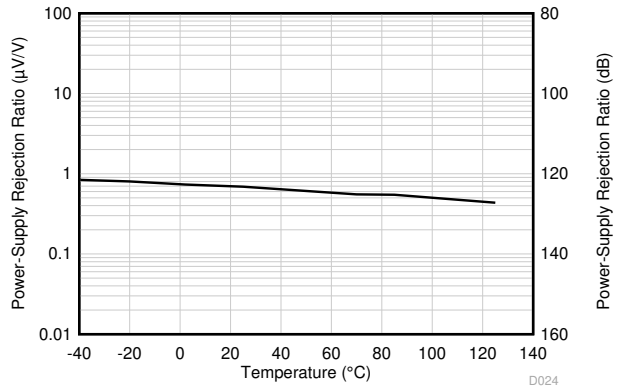


图 5-24. PSRR vs Temperature

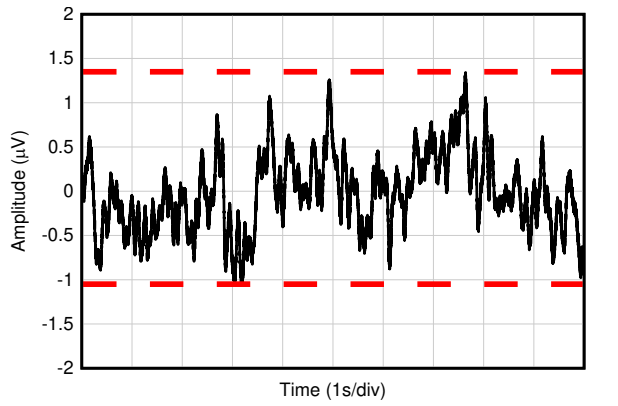


图 5-25. 0.1Hz to 10Hz Noise

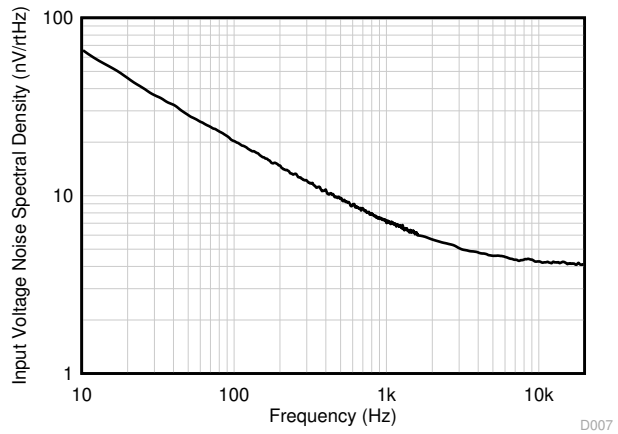
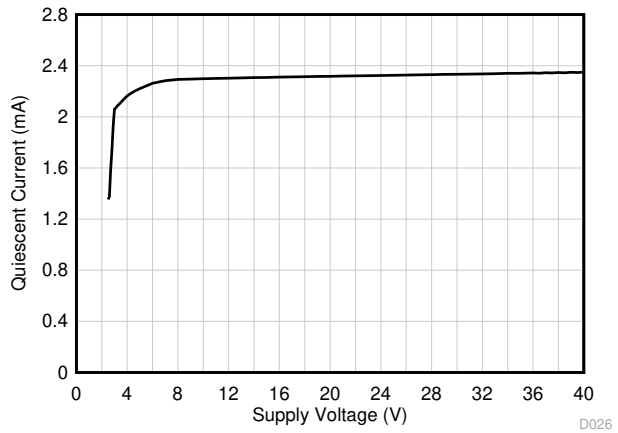


图 5-26. Input Voltage Noise Spectral Density vs Frequency

Copyright © 2024 Texas Instruments Incorporated

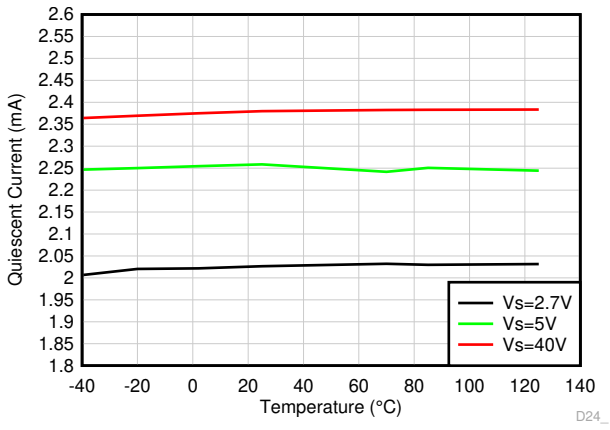
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



V_{CM} = V –

图 5-27. Quiescent Current vs Supply Voltage



V_{CM} = V –

图 5-28. Quiescent Current vs Temperature

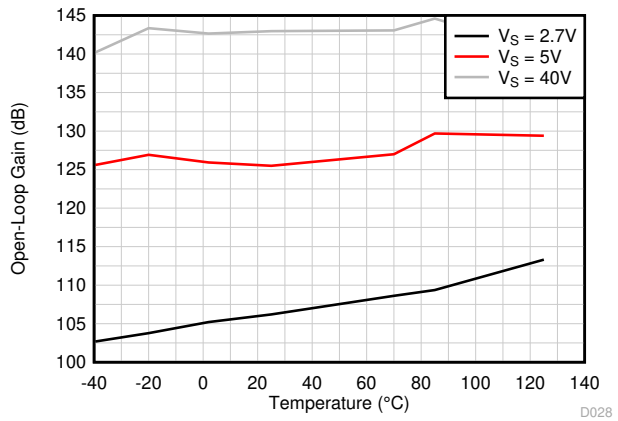


图 5-29. Open-Loop Voltage Gain vs Temperature (dB)

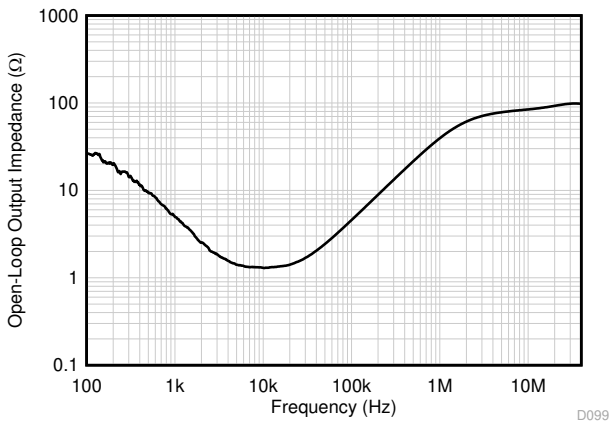
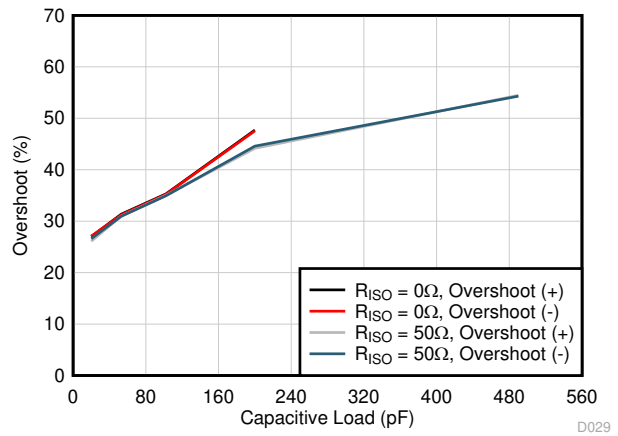
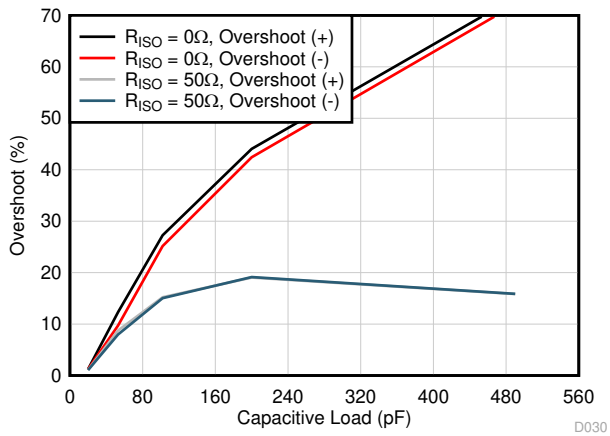


图 5-30. Open-Loop Output Impedance vs Frequency



20mV$_{pp}$ output step, G = – 1

图 5-31. Small-Signal Overshoot vs Capacitive Load



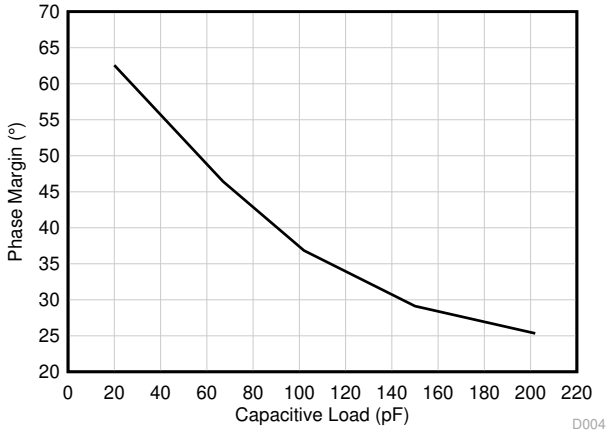
20mV$_{pp}$ output step, G = +1

图 5-32. Small-Signal Overshoot vs Capacitive Load

Copyright © 2024 Texas Instruments Incorporated

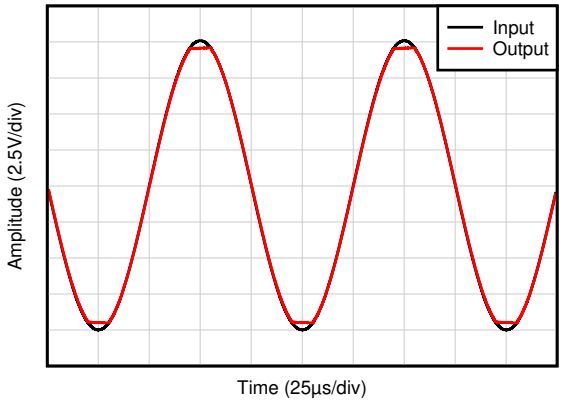
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



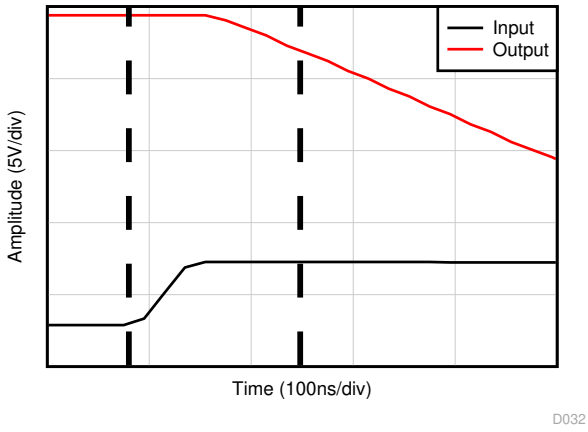
G = +1

图 5-33. Phase Margin vs Capacitive Load



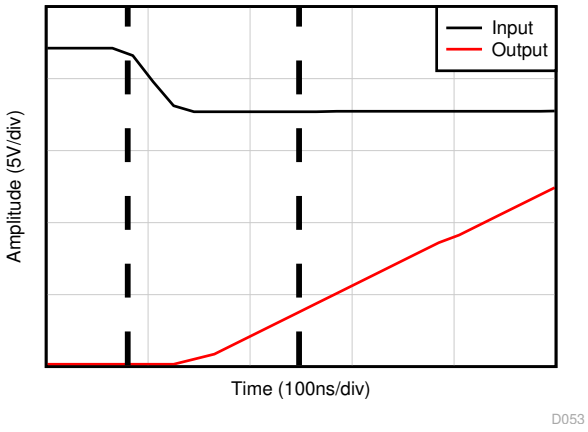
V_{IN} = ±10V_{pp}; V_S = V_{OUT} = ±9.55V

图 5-34. No Phase Reversal



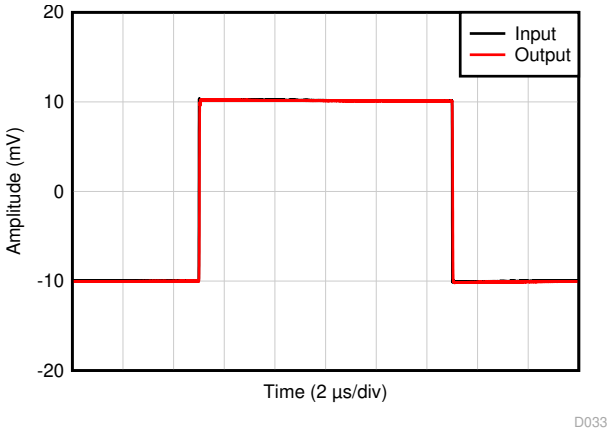
G = – 10

图 5-35. Positive Overload Recovery



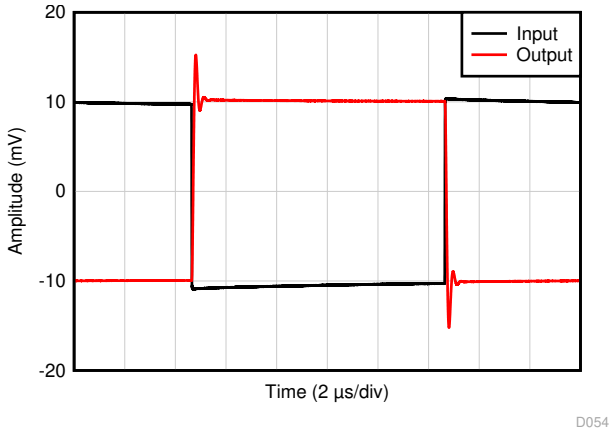
G = – 10

图 5-36. Negative Overload Recovery



C_L = 20pF, G = 1, 20mV_{pp} step response

图 5-37. Small-Signal Step Response



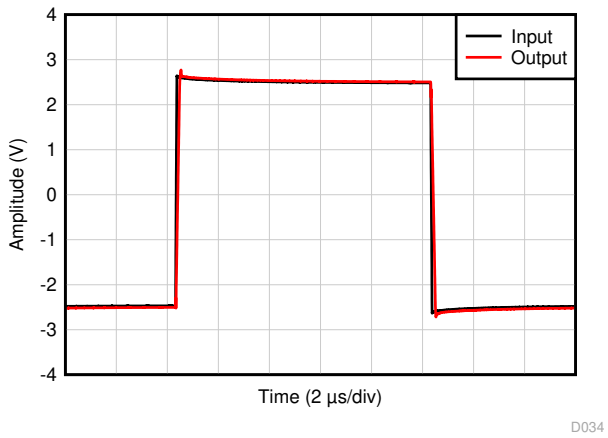
C_L = 20pF, G = – 1, 20mV_{pp} step response

图 5-38. Small-Signal Step Response

Copyright © 2024 Texas Instruments Incorporated

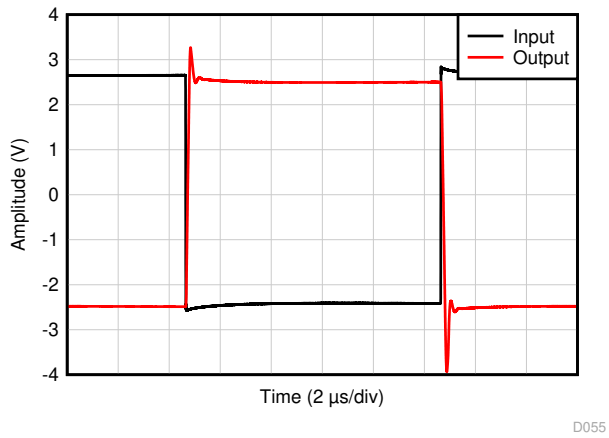
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



C_L = 20pF, G = 1, 5V_{pp} step response

图 5-39. Large-Signal Step Response



C_L = 20pF, G = –1, 5V_{pp} step response

图 5-40. Large-Signal Step Response

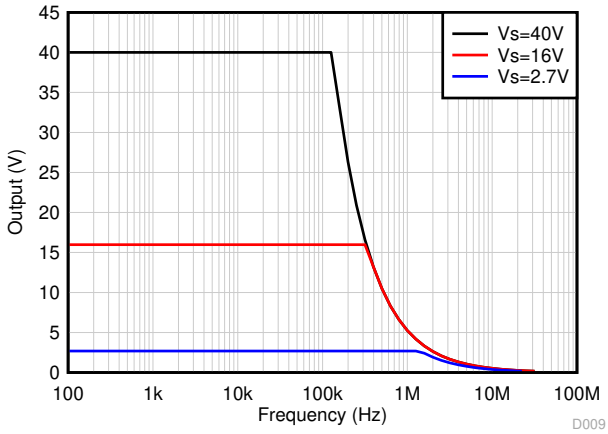


图 5-41. Maximum Output Voltage vs Frequency

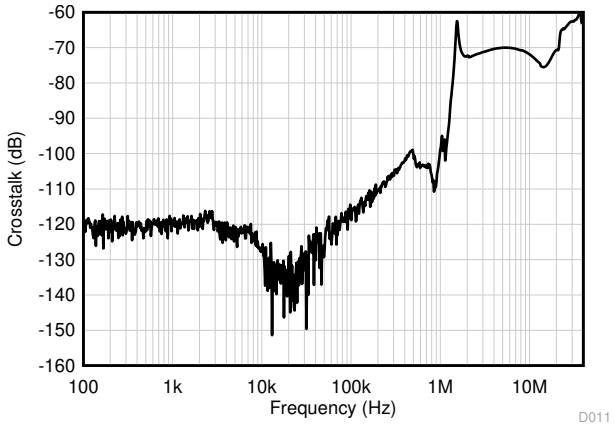


图 5-42. Channel Separation vs Frequency

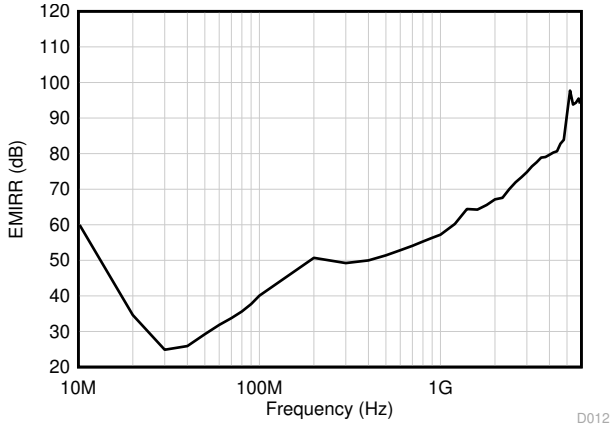


图 5-43. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

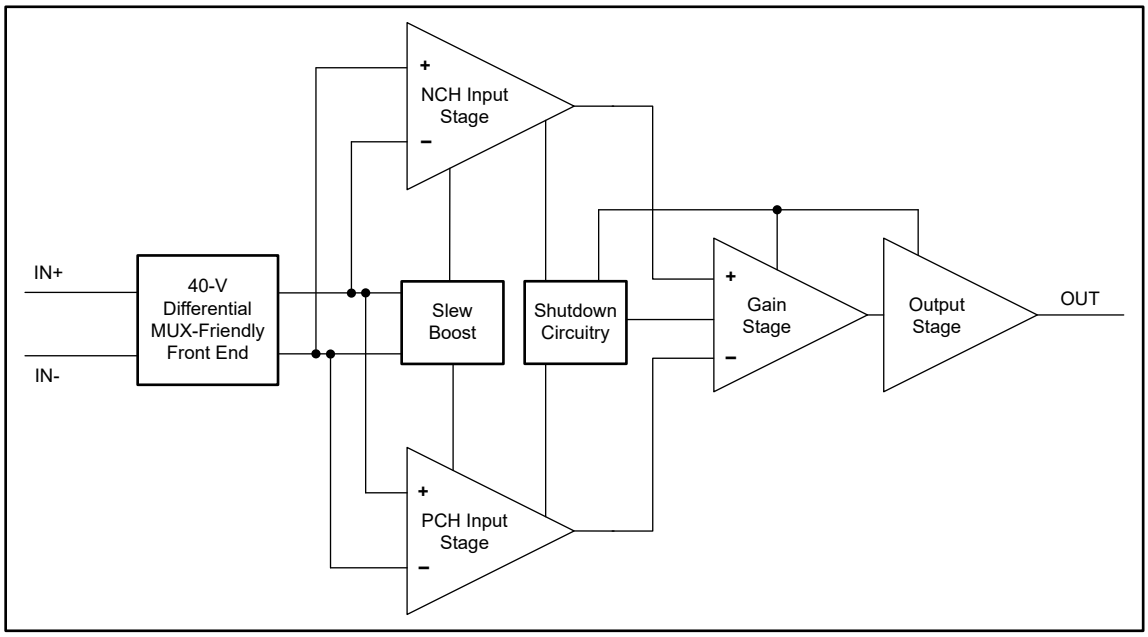
6.1 Overview

The OPAx992-Q1 family (OPA992-Q1, OPA2992-Q1, and OPA4992-Q1) is a family of high voltage (40V) general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input or output, low offset (±210µV, typical), and low offset drift (±0.25µV/°C, typical).

Special features such as differential and common-mode input voltage range to the supply rail, high short-circuit current (±65mA), and high slew rate (32V/µs) make the OPAx992-Q1 an extremely flexible, robust, and high-performance operational amplifier for high-voltage automotive applications.

6.2 Functional Block Diagram



Copyright © 2024 Texas Instruments Incorporated

6.3 Feature Description

6.3.1 Input Protection Circuitry

The OPAx992-Q1 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. 图 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in 图 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

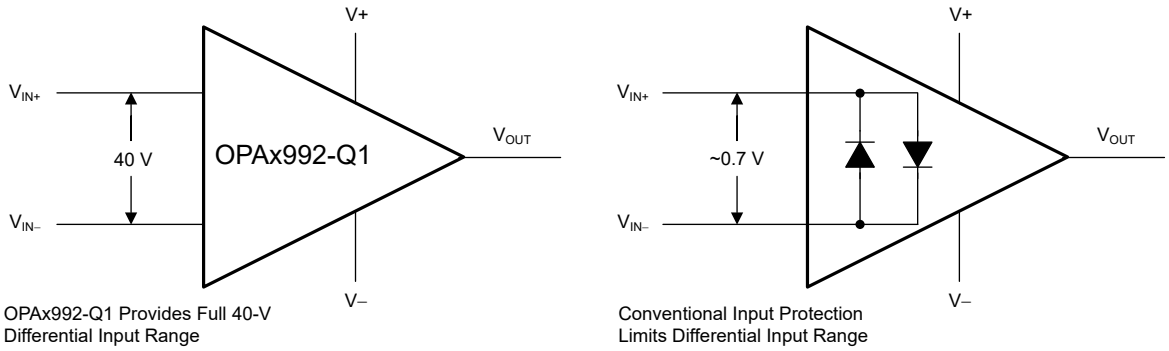


图 6-1. OPAx992-Q1 Input Protection Does Not Limit Differential Input Capability

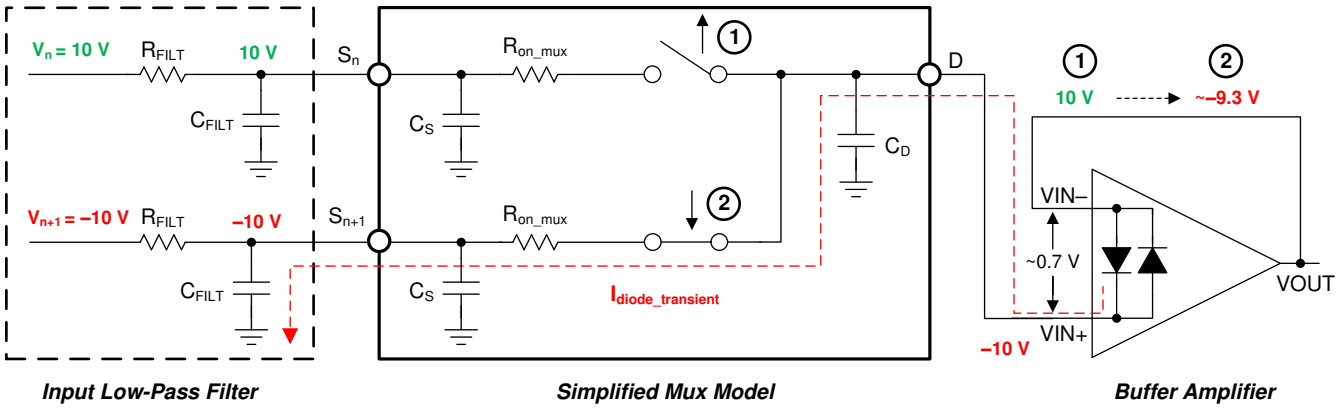


图 6-2. Back-to-Back Diodes Create Settling Issues

The OPAx992-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an excellent op amp for multichannel, high-switched, input applications. The OPAx992-Q1 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40V, making the device designed for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

Copyright © 2024 Texas Instruments Incorporated

6.3.2 EMI Rejection

The OPAx992-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx992-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. 图 6-3 shows the results of this testing on the OPAx992-Q1. 表 6-1 provides the EMIRR IN+ values for the OPAx992-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance relating to op amps and is available for download from www.ti.com.

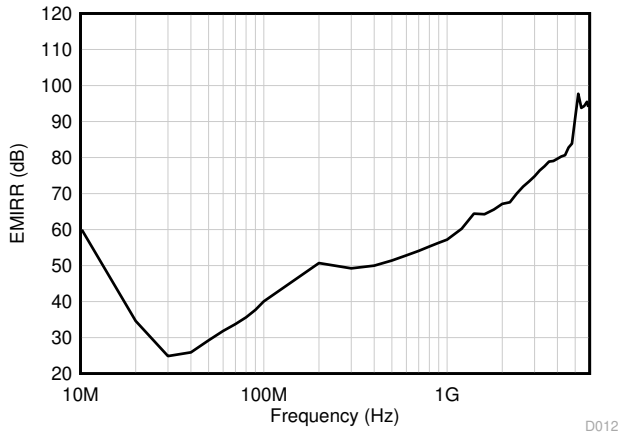


图 6-3. EMIRR Testing

表 6-1. OPAx992-Q1 EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	56.3dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	65.6dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	91.0dB

Copyright © 2024 Texas Instruments Incorporated

6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx992-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx992-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. 图 6-4 shows an application example for the OPA2992-Q1 that has significant self heating because of the power dissipation (0.954W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 55°C, the device junction temperature reaches 180°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. 图 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, then the amplifier oscillates between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the SOIC (8) package.

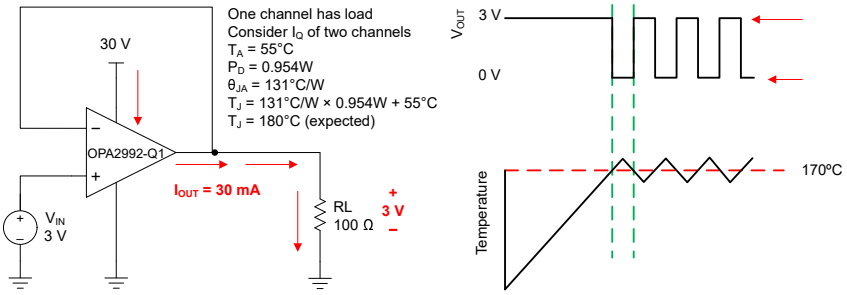


图 6-4. Thermal Protection

6.3.4 Capacitive Load and Stability

The OPAx992-Q1 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see 图 6-5 and 图 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier are stable in operation.

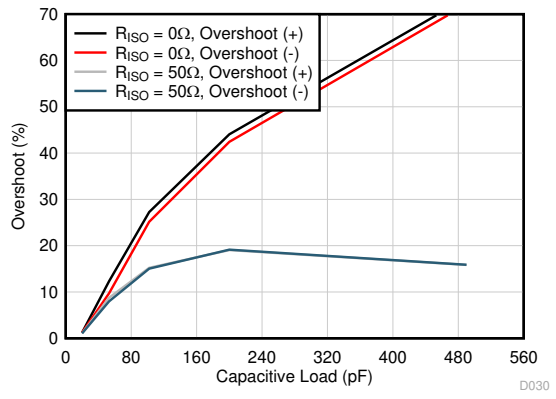


图 6-5. Small-Signal Overshoot vs Capacitive Load ($20mV_{pp}$ Output Step, G = +1)

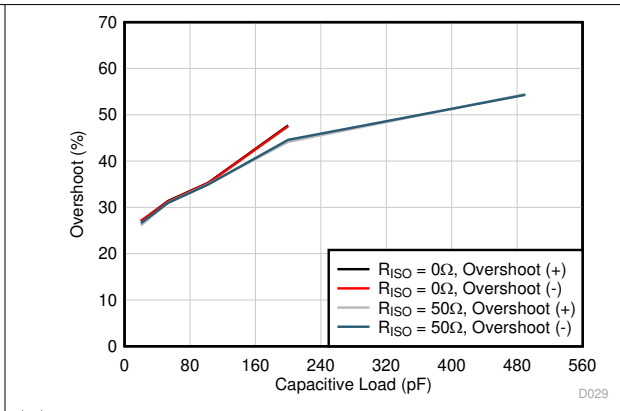


图 6-6. Small-Signal Overshoot vs Capacitive Load ($20mV_{pp}$ Output Step, G = -1)

Copyright © 2024 Texas Instruments Incorporated

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in 图 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx992-Q1 an excellent choice for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in 图 6-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

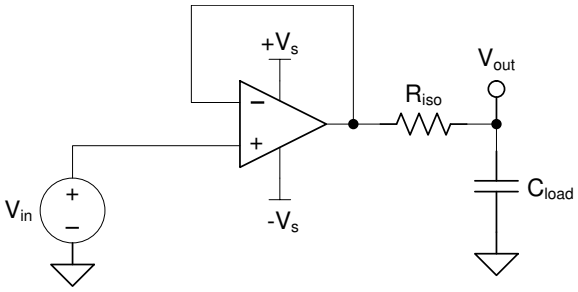


图 6-7. Extending Capacitive Load Drive With the OPA992-Q1

Copyright © 2024 Texas Instruments Incorporated

6.3.5 Common-Mode Voltage Range

The OPAx992-Q1 is a 40V, true rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in 图 6-8. The N-channel pair is active for input voltages close to the positive rail, typically from (V+) – 1V to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V, in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region.

图 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

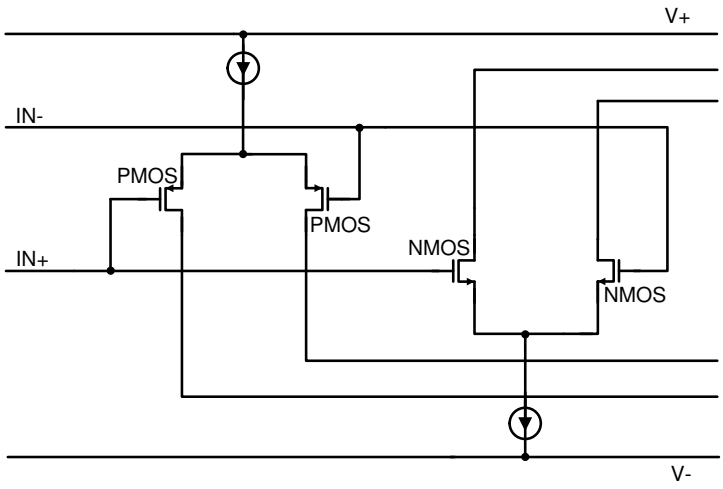


图 6-8. Rail-to-Rail Input Stage

6.3.6 Phase Reversal Protection

The OPAx992-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx992-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. 图 6-9 shows this performance. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

Copyright © 2024 Texas Instruments Incorporated

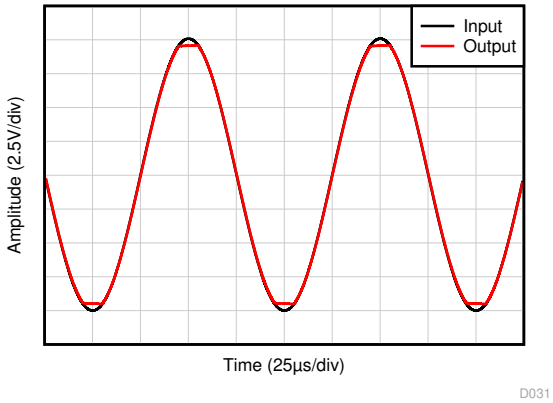


图 6-9. No Phase Reversal

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 6-10 shows the ESD circuits contained in the OPAx992-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Copyright © 2024 Texas Instruments Incorporated

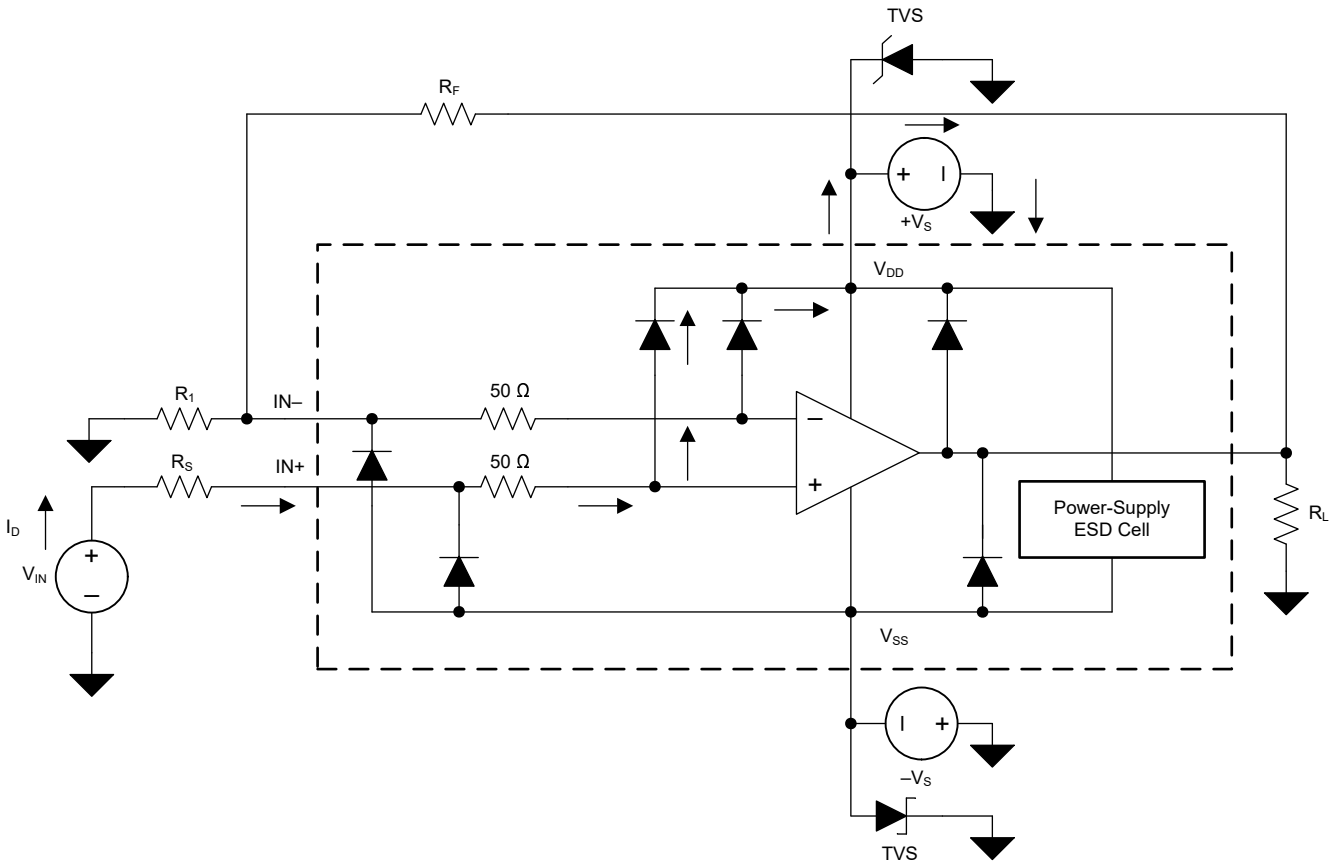


图 6-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example, 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

Copyright © 2024 Texas Instruments Incorporated

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx992-Q1 is approximately 170ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the desired value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions, and circuit designers can leverage this information to guardband systems, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

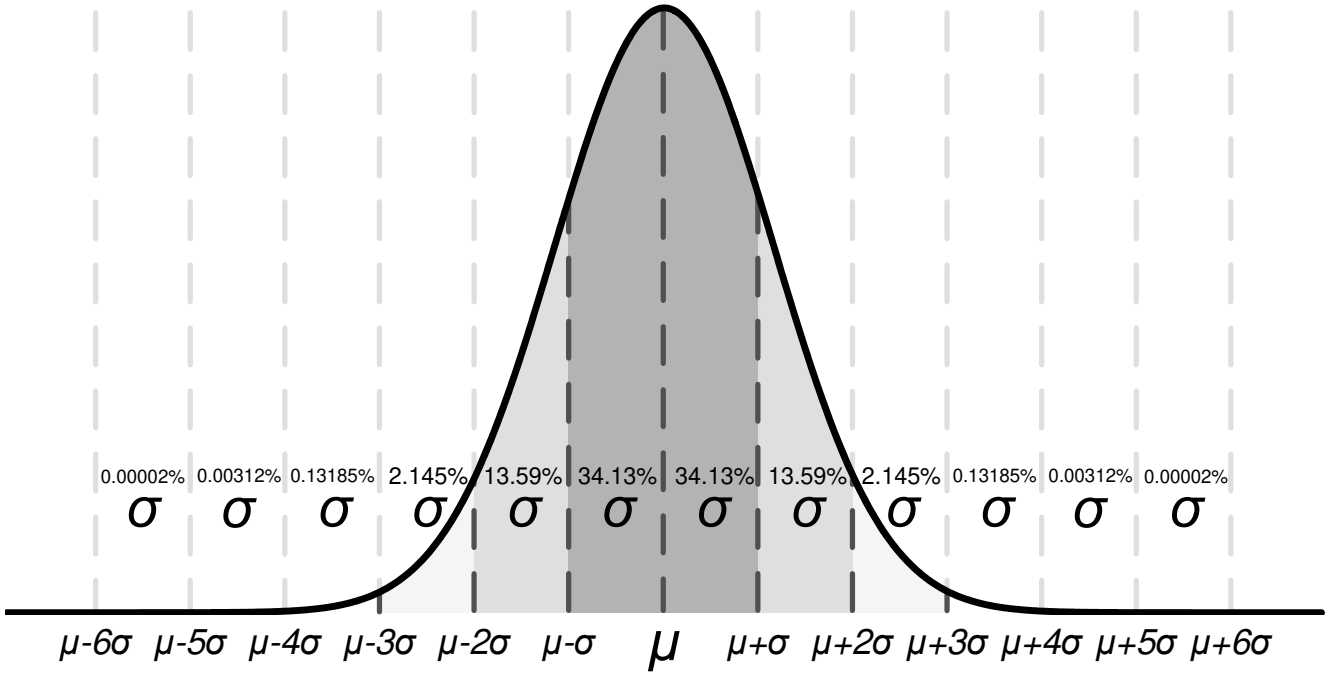


图 6-11. Ideal Gaussian Distribution

图 6-11 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) to most accurately represent the typical value.

Copyright © 2024 Texas Instruments Incorporated

This chart can be used to calculate approximate probability of a specification in a unit; for example, for OPAx992-Q1, the typical input voltage offset is 210µV. So 68.2% of all OPAx992-Q1 devices are expected to have an offset from –210µV to +210µV. At 4 σ (±840µV), 99.9937% of the distribution has an offset voltage less than ±840µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits are removed from production material. For example, the OPAx992-Q1 family has a maximum offset voltage of 1mV at 25°C, and even though this corresponds to slightly less than 5 σ (≅1 in 1.7 million units), which is extremely unlikely, TI maintains that any unit with larger offset than 1mV is removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6 σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and can be an option as a wide guardband to design a system around. In this case, the OPAx992-Q1 family does not have a maximum or minimum for offset voltage drift. But based on the typical value of 0.25µV/°C in the *Electrical Characteristics* table, the 6 σ value for offset voltage drift is about 1.5µV/°C when calculated. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

Note that process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot verify the performance of a device. This information must be used only to estimate the performance of a device.

6.4 Device Functional Modes

The OPAx992-Q1 has a single functional mode and is operational when the power-supply voltage is greater than or equal to 2.7V (±1.35V). The maximum power supply voltage for the OPAx992-Q1 is 40V (±20V).

Copyright © 2024 Texas Instruments Incorporated

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPAx992-Q1 family offers excellent DC precision and AC performance. These devices operate up to 40V supply rails and offer true rail-to-rail input or output, low offset voltage and offset voltage drift, as well as 10.6MHz bandwidth and high output drive. These features make the OPAx992-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

图 7-1 shows the OPA992-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in 图 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution* .

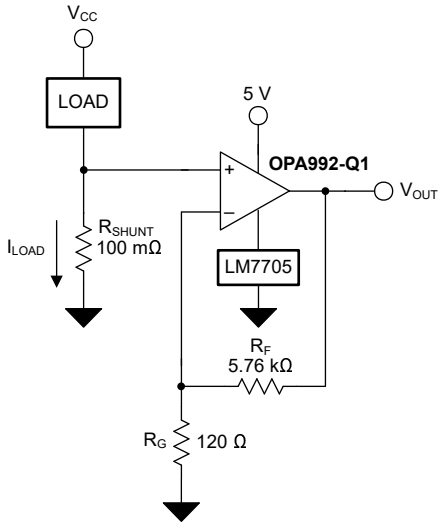


图 7-1. OPAx992-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 7-1 is given in 方程式 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

Copyright © 2024 Texas Instruments Incorporated

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using 方程式 2:

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using 方程式 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the OPA992-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the OPA992-Q1 to produce the necessary output voltage is calculated using 方程式 3:

$$Gain = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using 方程式 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. 方程式 4 is used to size the resistors, R_F and R_G, to set the gain of the OPA992-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because the values are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors generate thermal noise that exceeds the intrinsic noise of the op amp. 图 7-2 shows the measured transfer function of the circuit shown in 图 7-1.

7.2.1.3 Application Curve

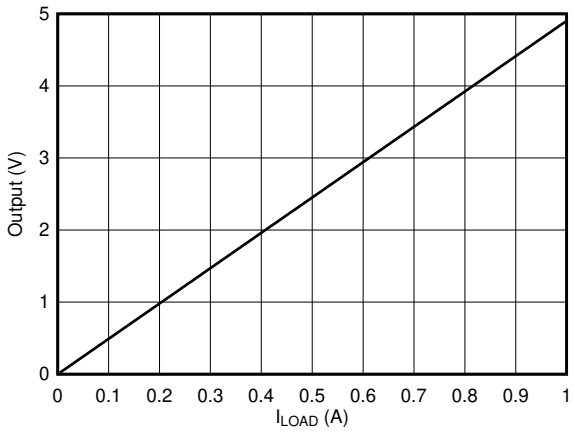


图 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The OPAx992-Q1 is specified for operation from 2.7V to 40V (±1.35V to ±20V); many specifications apply from –40°C to 125°C or with specific supply voltages and test conditions.

> **小心**
>
> Supply voltages larger than 40V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout* .

Copyright © 2024 Texas Instruments Incorporated

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and through the op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

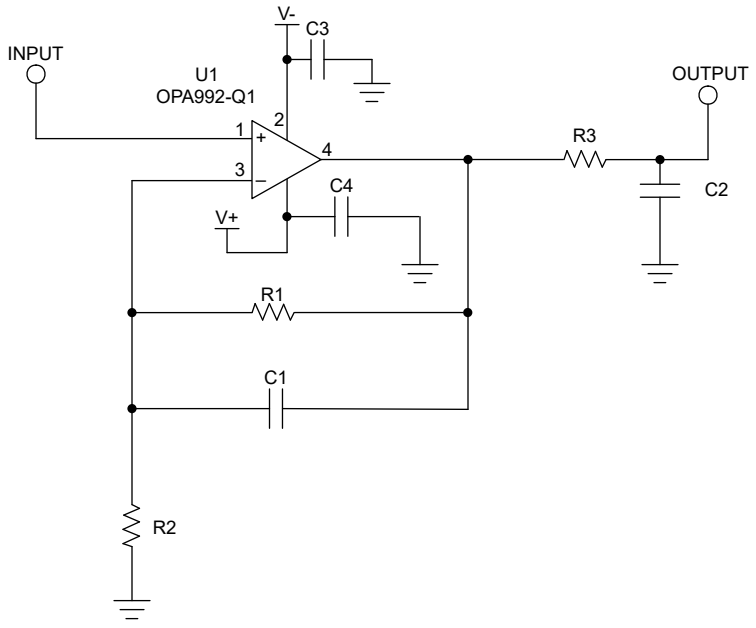


图 7-3. Schematic for Noninverting Configuration Layout Example

Copyright © 2024 Texas Instruments Incorporated

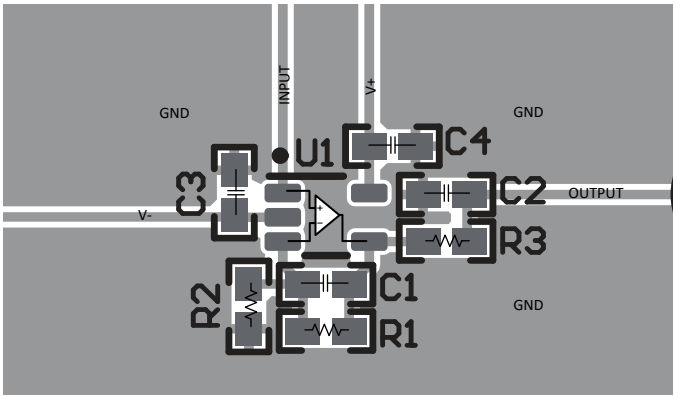


图 7-4. Operational Amplifier Board Layout for Noninverting Configuration - SC70 (DCK) Package

Copyright © 2024 Texas Instruments Incorporated

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

备注

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note
- Texas Instruments, *0A to 1A, Single-Supply, Low-Side, Current Sensing Solution* reference design (TIPD129)

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.5 Trademarks

TINA-TI™ is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

8.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Copyright © 2024 Texas Instruments Incorporated

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (April 2023) to Revision E (July 2024)	Page
• 向*封装信息* 表中添加了 8 引脚 TSSOP (PW) 封装	1
• Added 8-pin TSSOP (PW) package to the *Pin Configurations and Functions* section	3
• Added 8-pin TSSOP (PW) package to Thermal Information for Dual Channel table	7

Changes from Revision C (February 2023) to Revision D (April 2023)	Page
• 将 14 引脚 SOIC (D) 和 TSSOP (PW) 封装的状态从*预发布* 更改为*正在供货*	1

Changes from Revision B (January 2023) to Revision C (February 2023)	Page
• 将 5 引脚 SOT-23 和 8 引脚 SOIC 封装的状态从*预发布* 更改为*正在供货*	1

Changes from Revision A (December 2022) to Revision B (January 2023)	Page
• 删除了 SC70-5 (DCK) 封装的预发布标签	1

Changes from Revision * (August 2022) to Revision A (December 2022)	Page
• 将器件状态从*预告信息* 更改为 *ProdMix*	1
• 删除了 VSSOP-8 (DGK) 封装的预发布标签	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2992QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S4T
OPA2992QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S4T
OPA2992QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992Q
OPA2992QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2992Q
OPA2992QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2992PW
OPA2992QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2992PW
OPA4992QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4992QD
OPA4992QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4992QD
OPA4992QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q4992PW
OPA4992QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q4992PW
OPA992QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2VWH
OPA992QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2VWH
OPA992QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NH
OPA992QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2992-Q1, OPA4992-Q1, OPA992-Q1 :

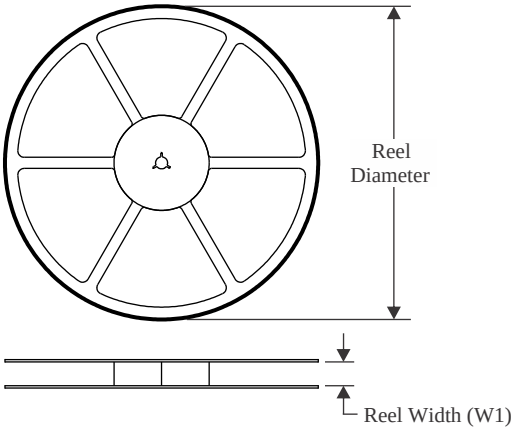
- Catalog : OPA2992, OPA4992, OPA992

NOTE: Qualified Version Definitions:

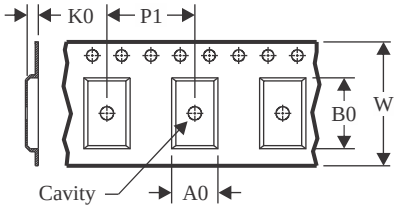
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

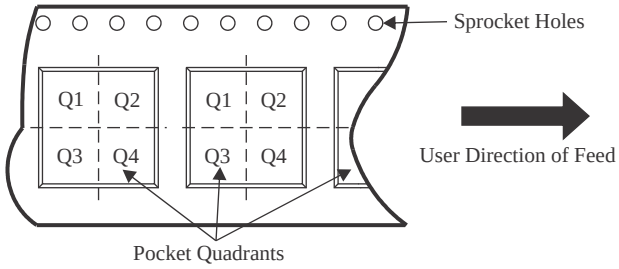


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

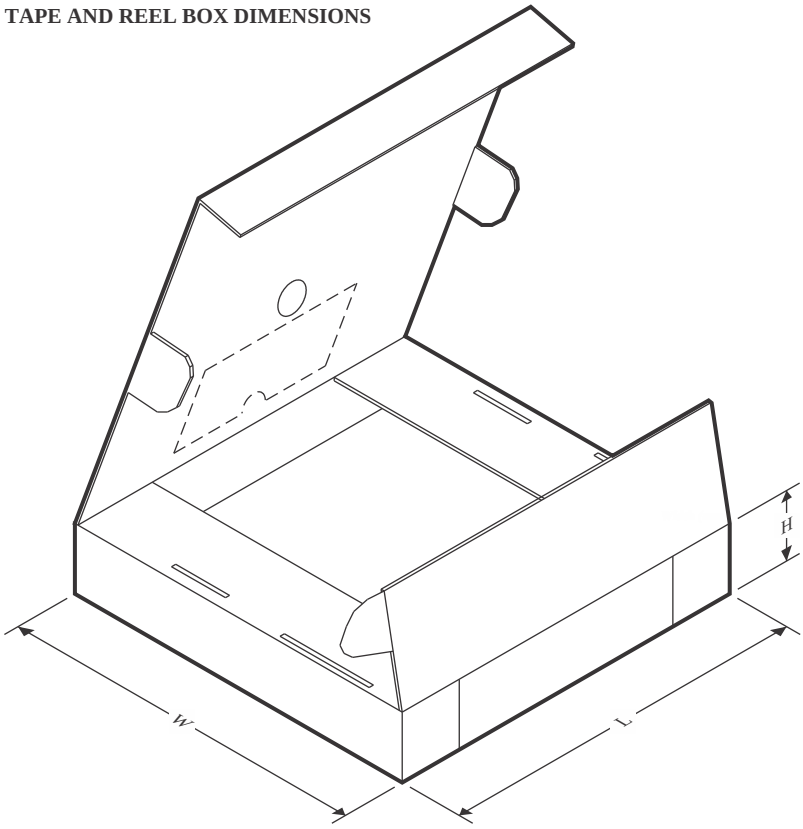
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2992QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2992QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2992QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
OPA4992QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4992QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA992QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA992QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

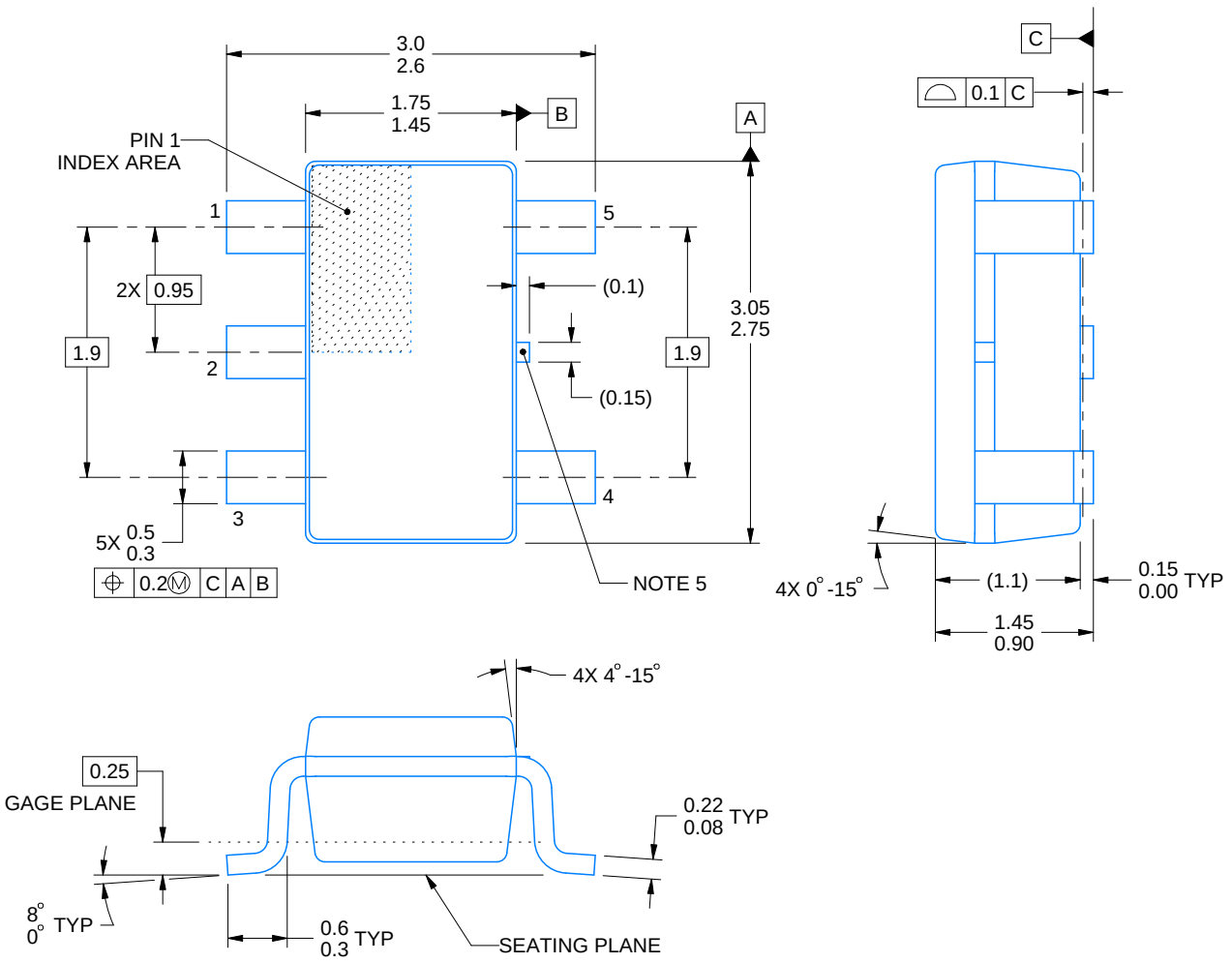
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2992QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2992QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
OPA2992QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
OPA4992QDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
OPA4992QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
OPA992QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA992QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

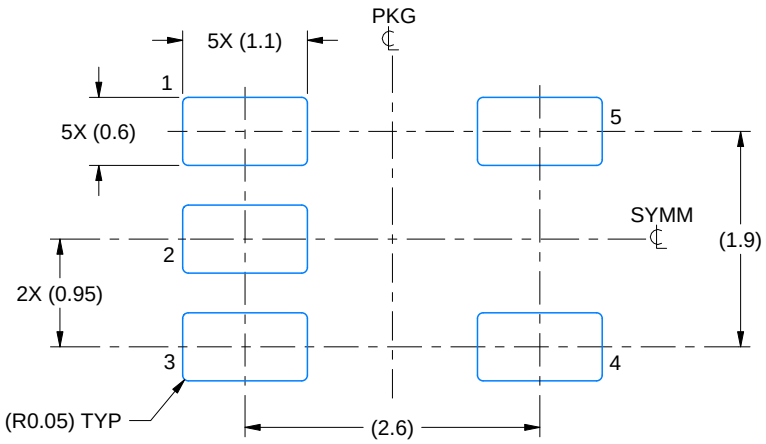
SMALL OUTLINE TRANSISTOR



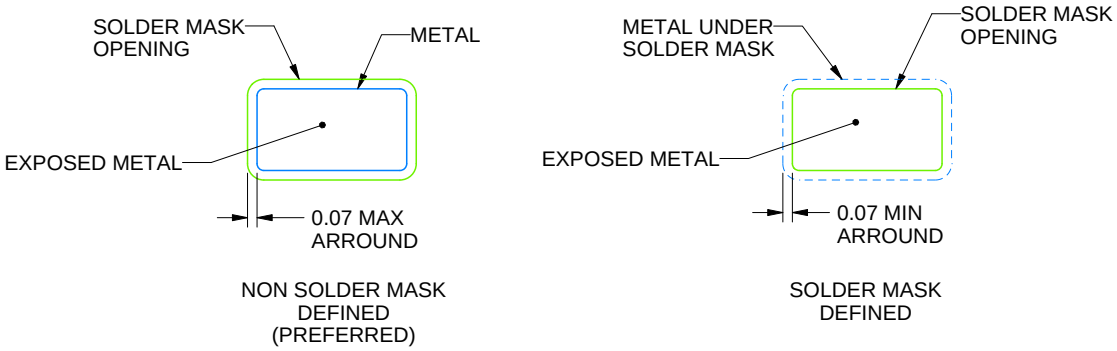
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

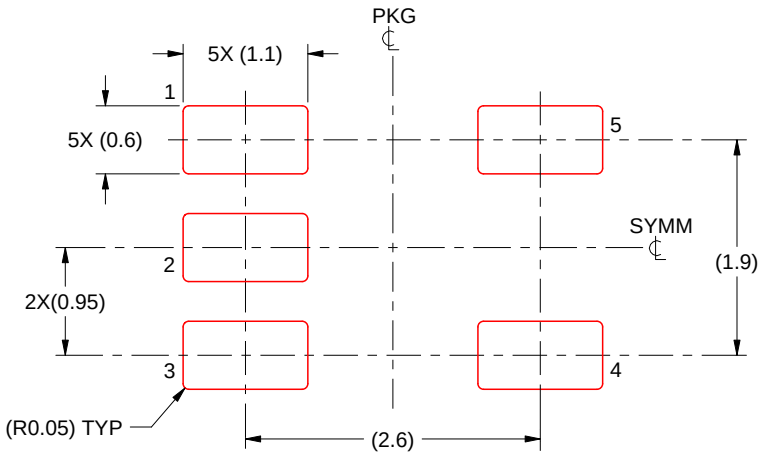


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

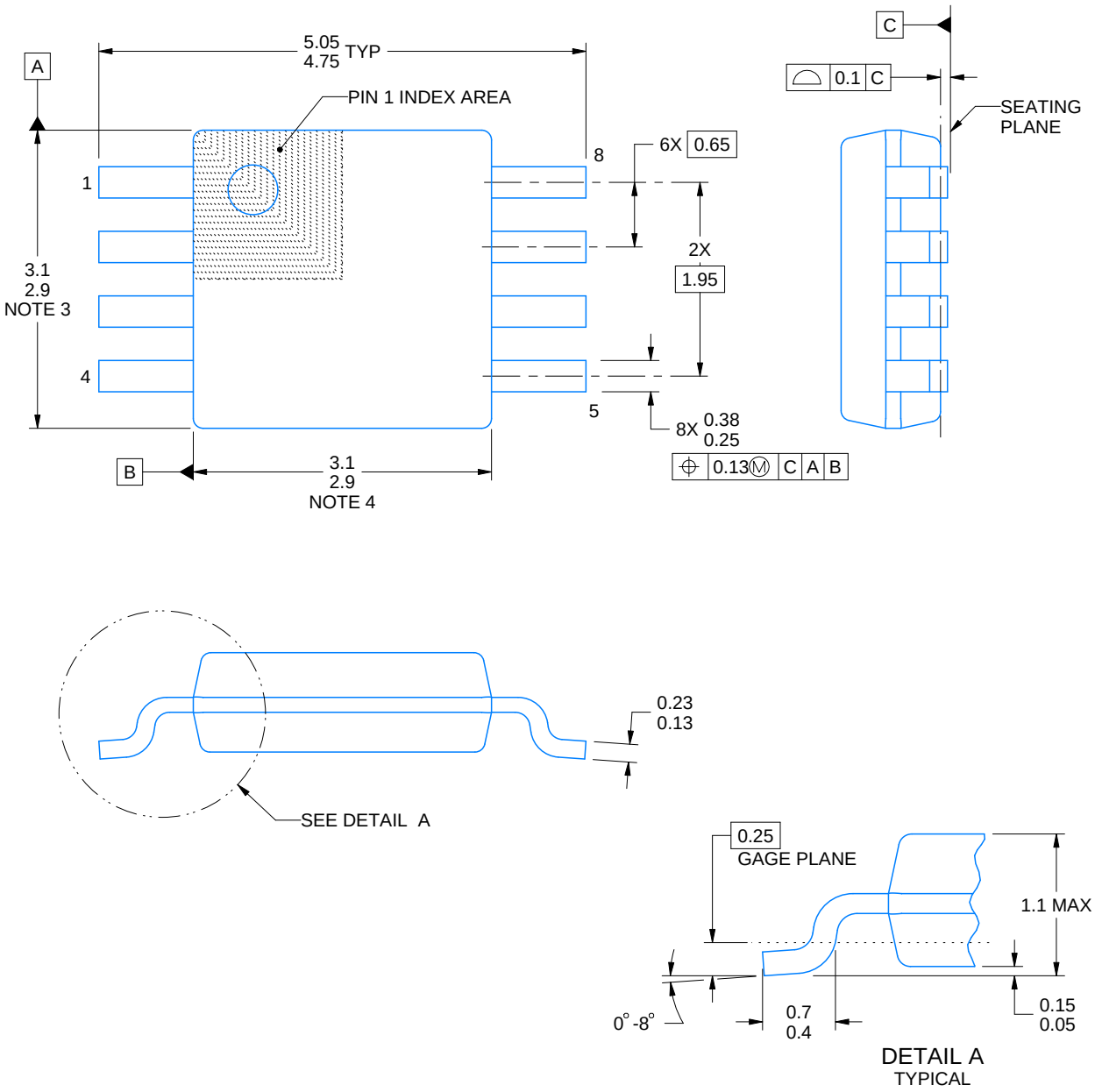
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

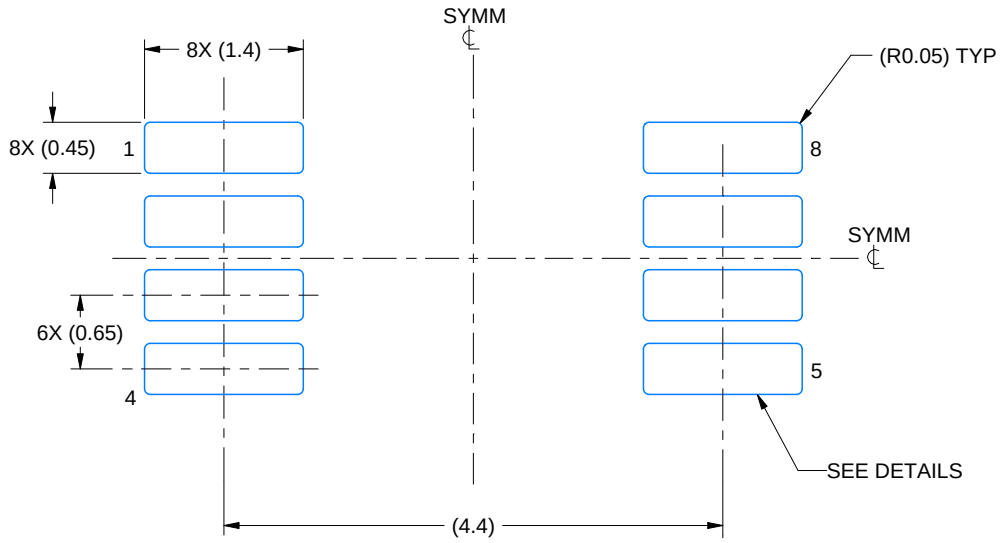
SMALL OUTLINE PACKAGE



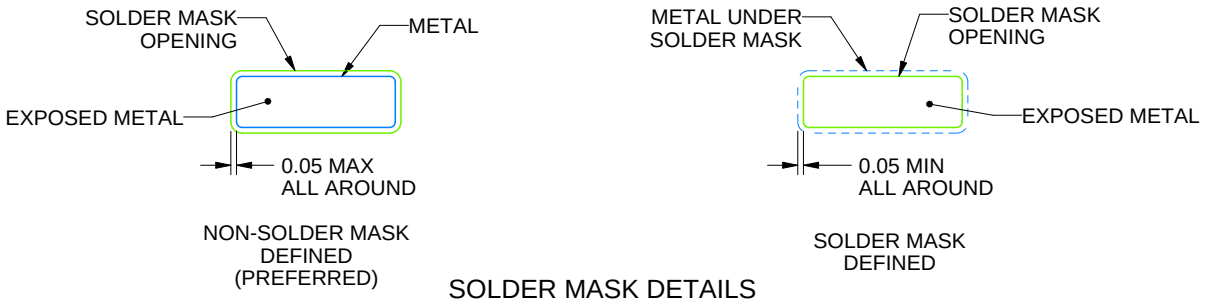
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

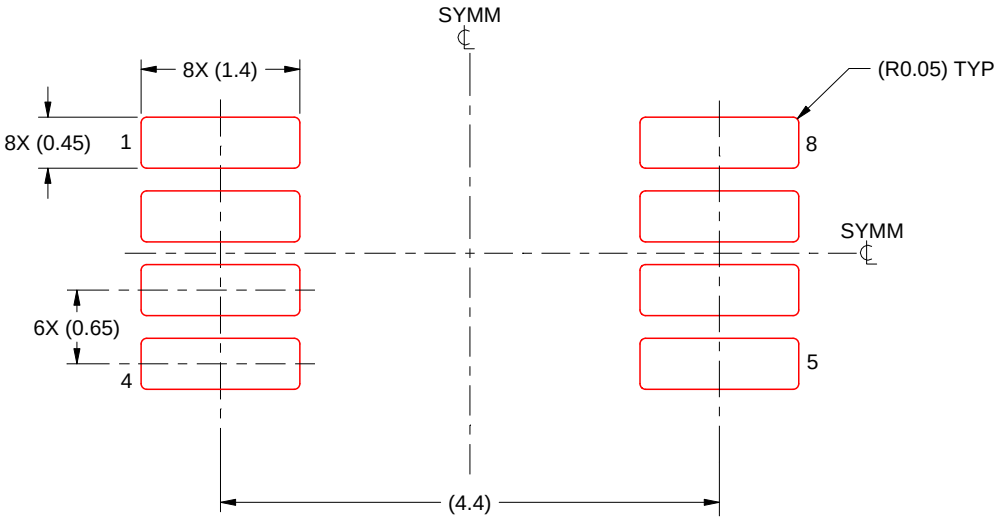


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

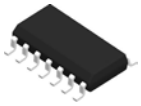


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

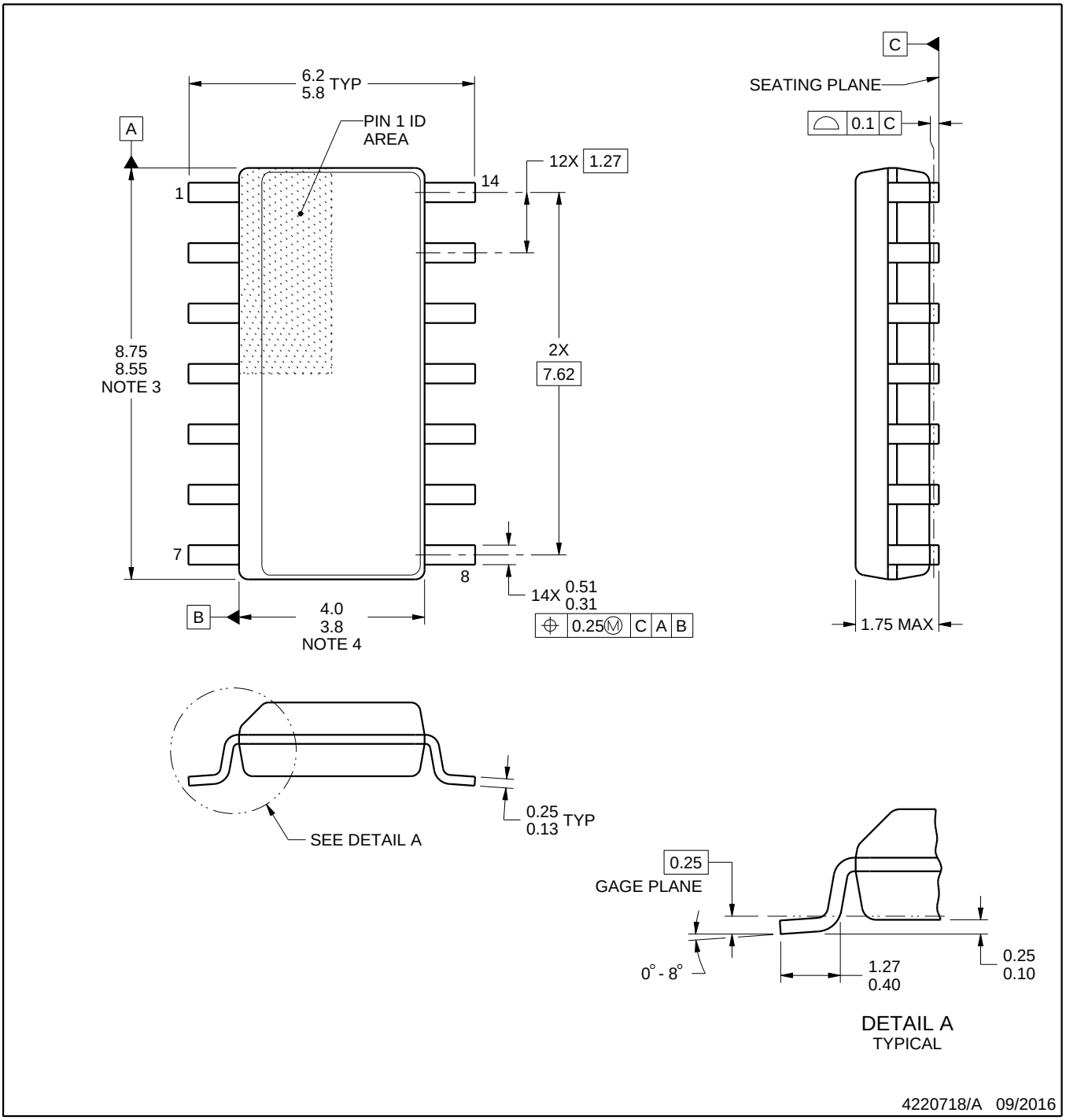


PACKAGE OUTLINE

D0014A

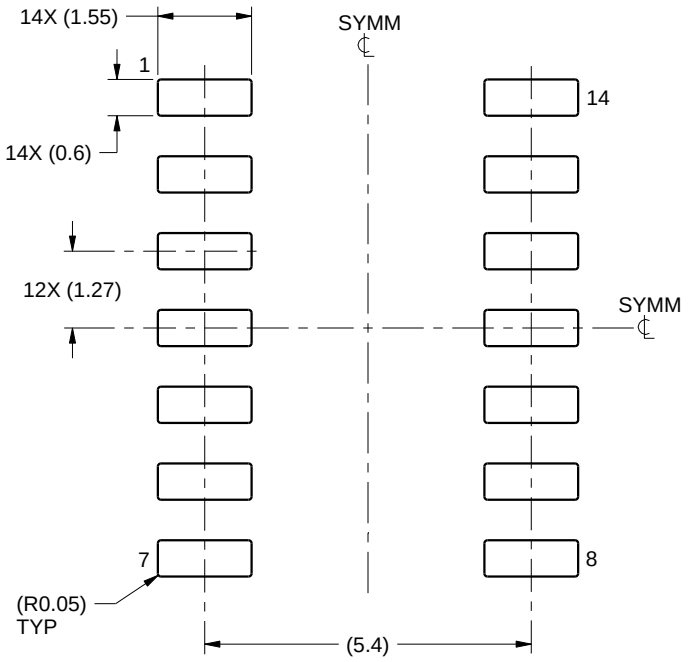
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

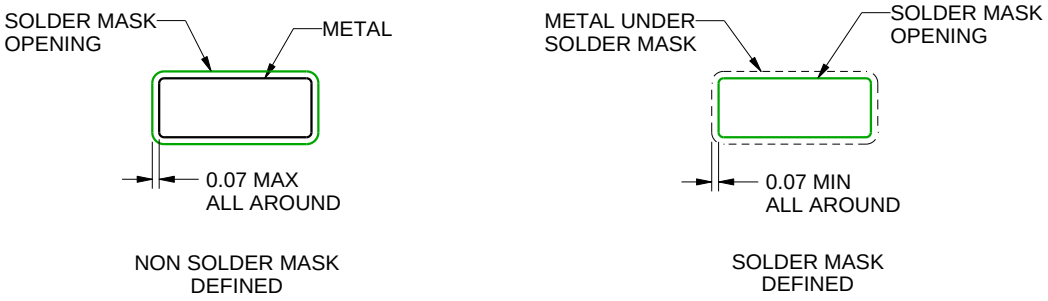


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

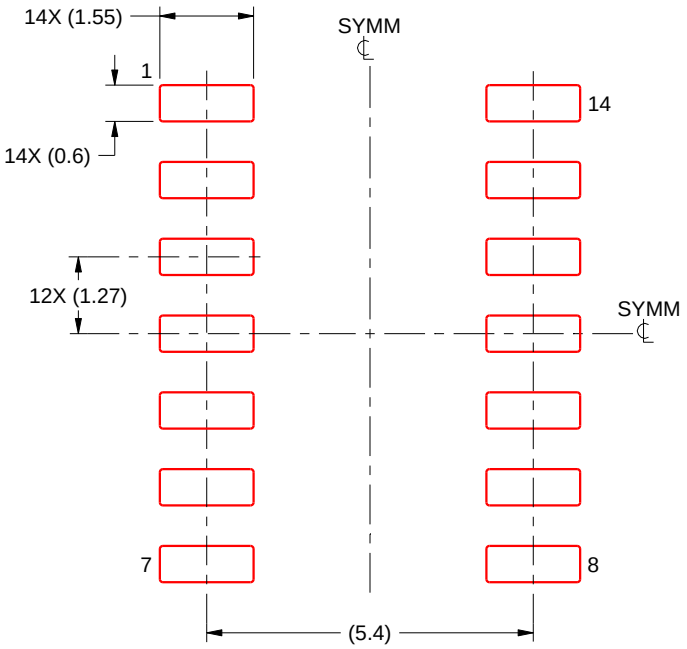
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

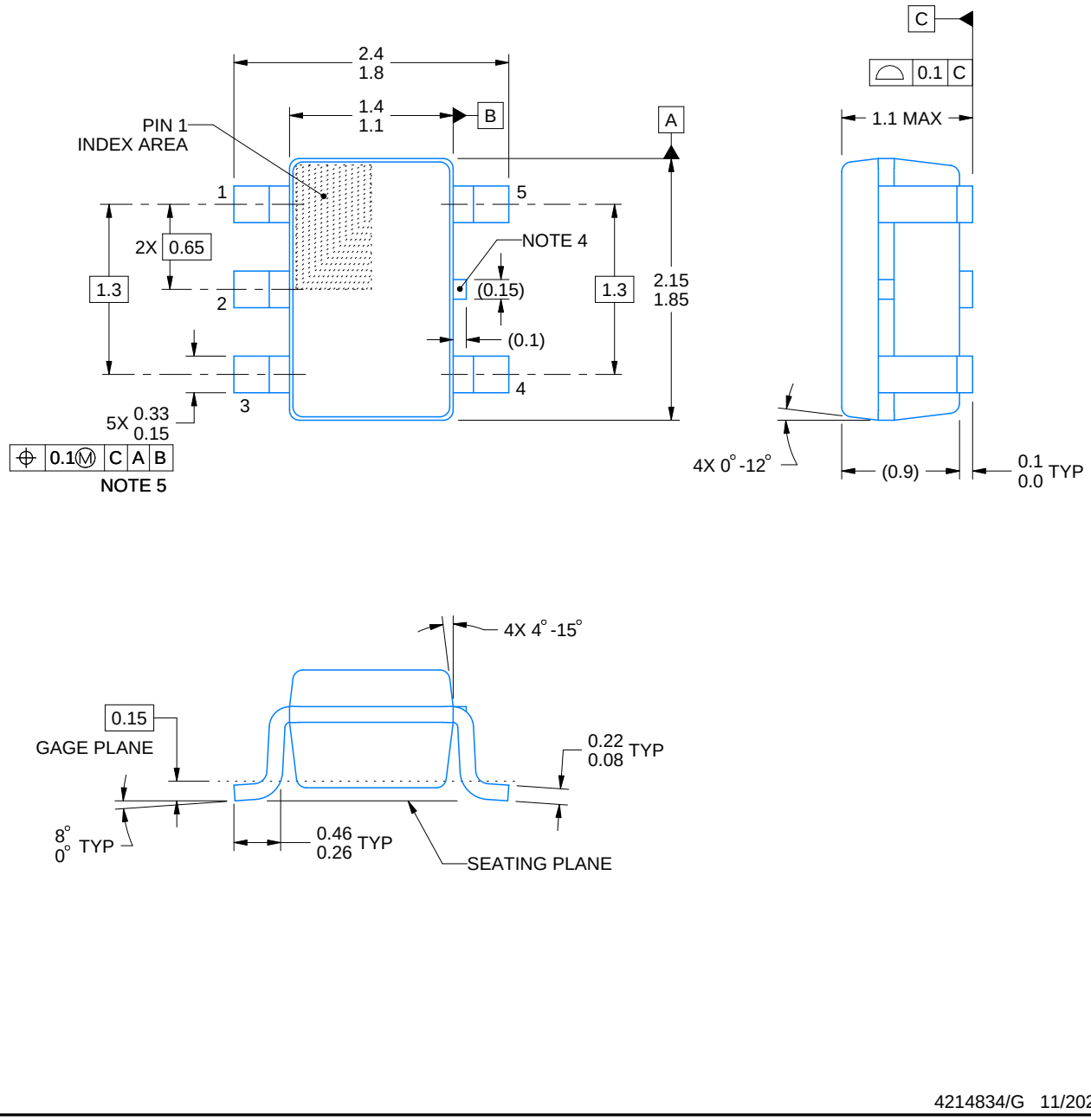
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

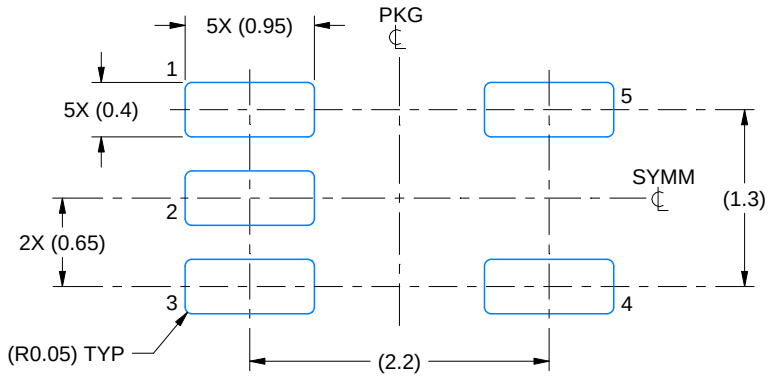
SMALL OUTLINE TRANSISTOR



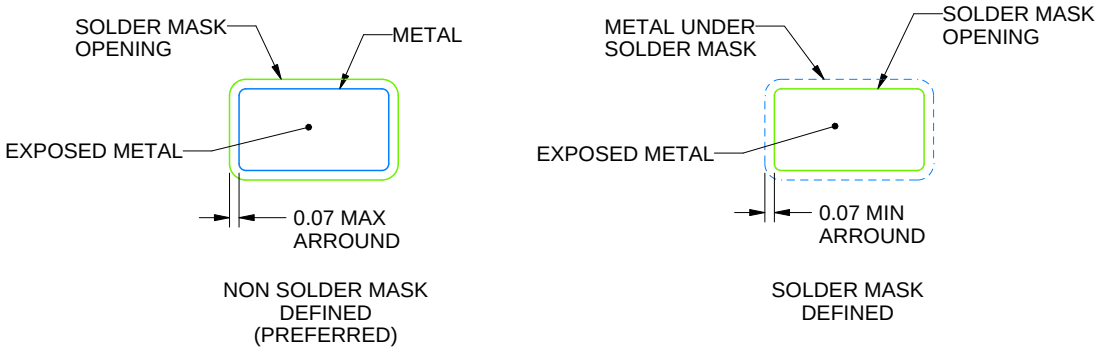
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

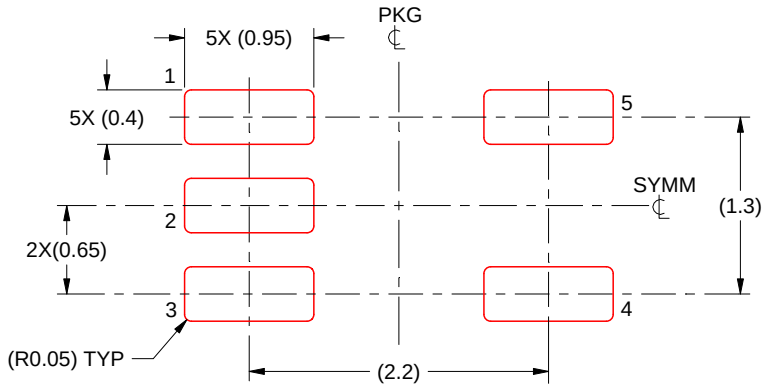


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

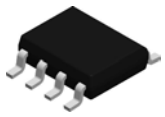


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

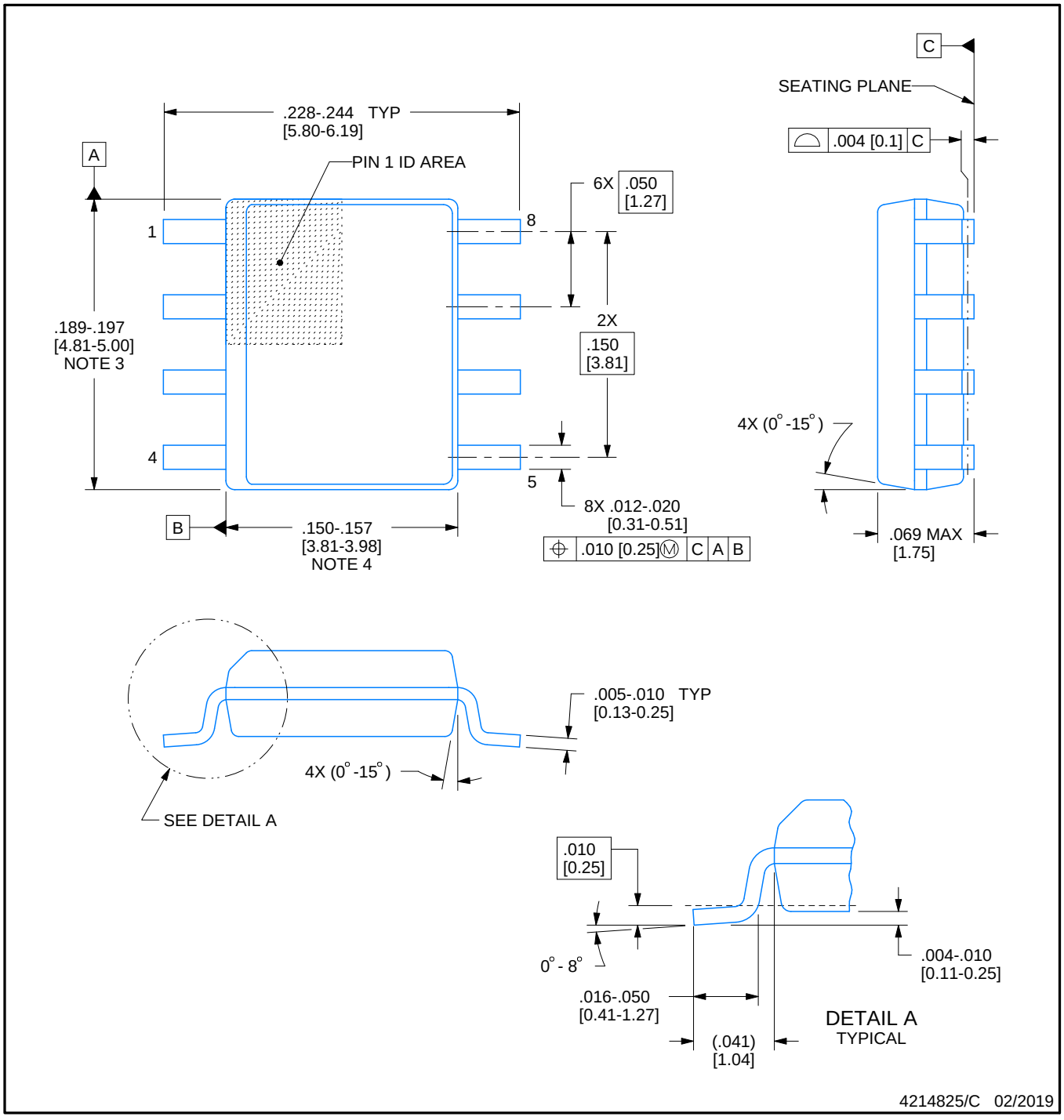


PACKAGE OUTLINE

D0008A

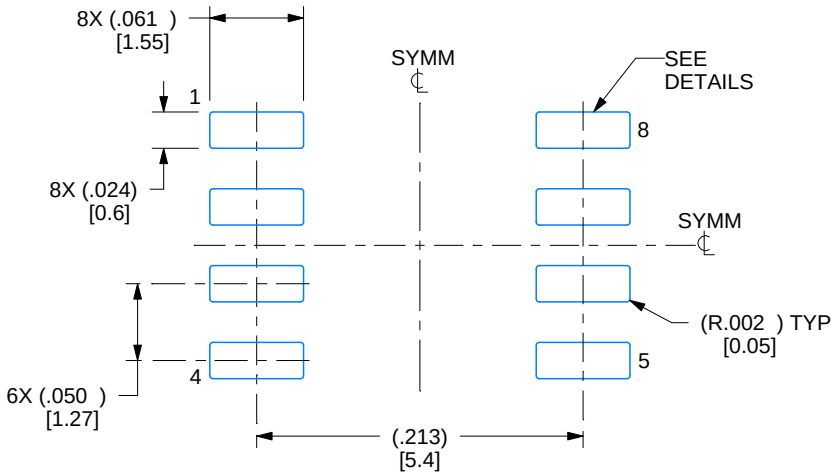
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

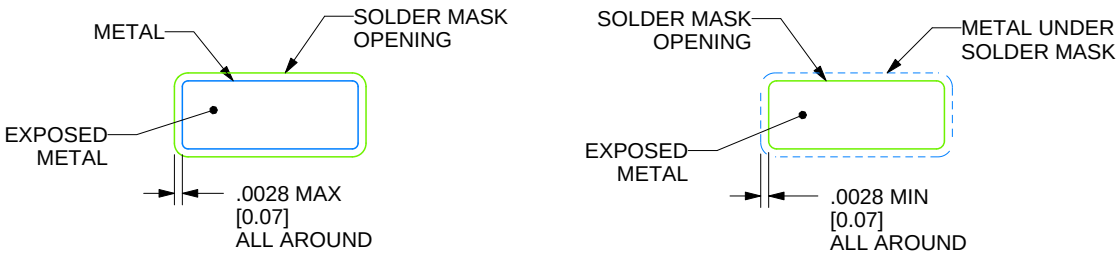


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

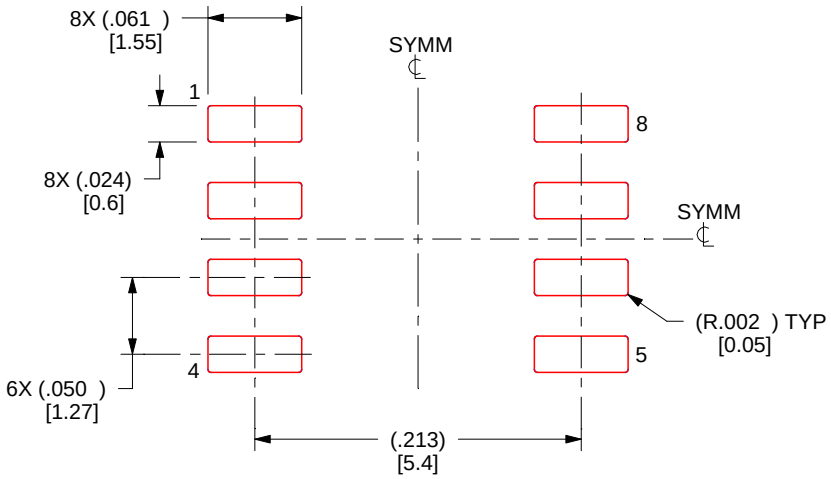
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

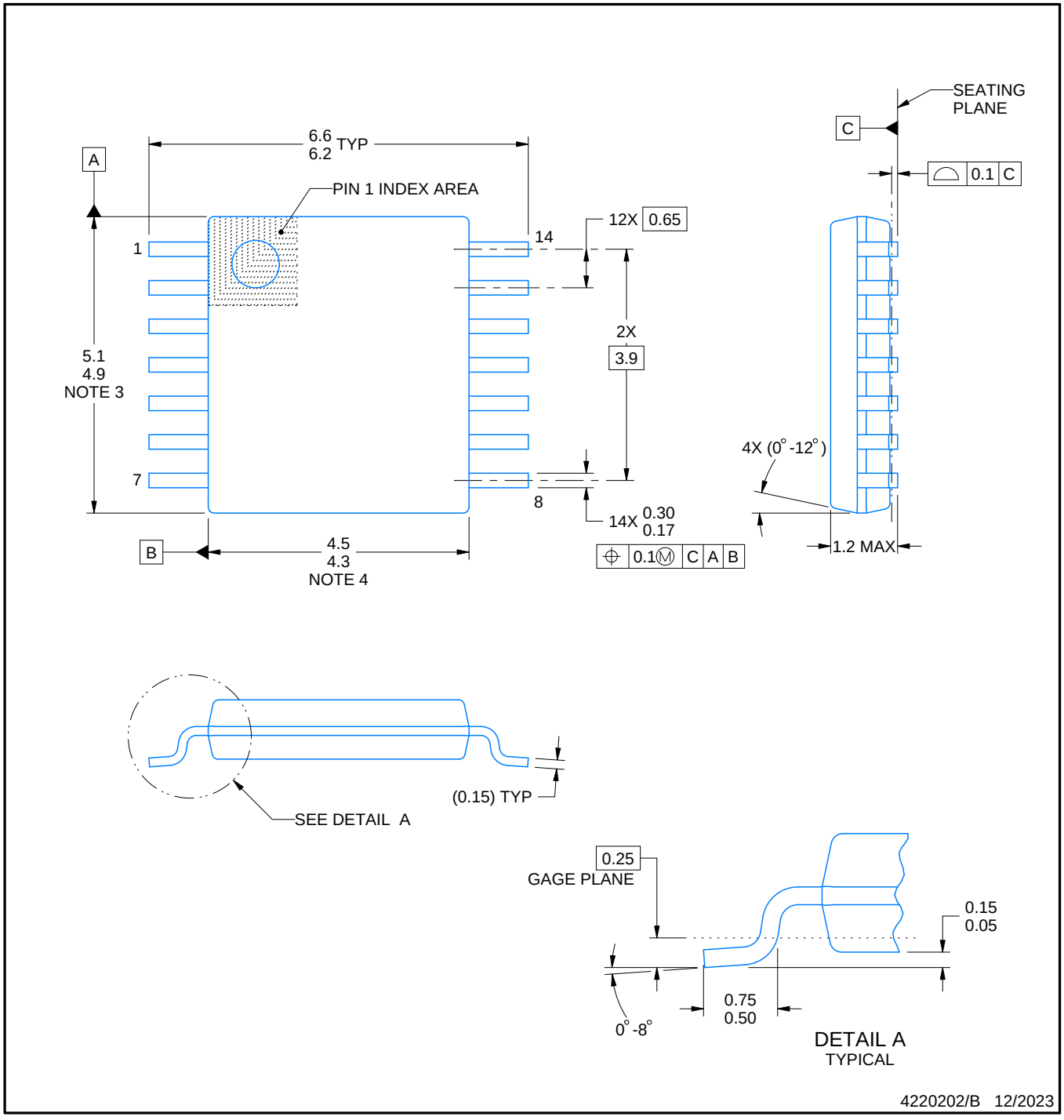
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

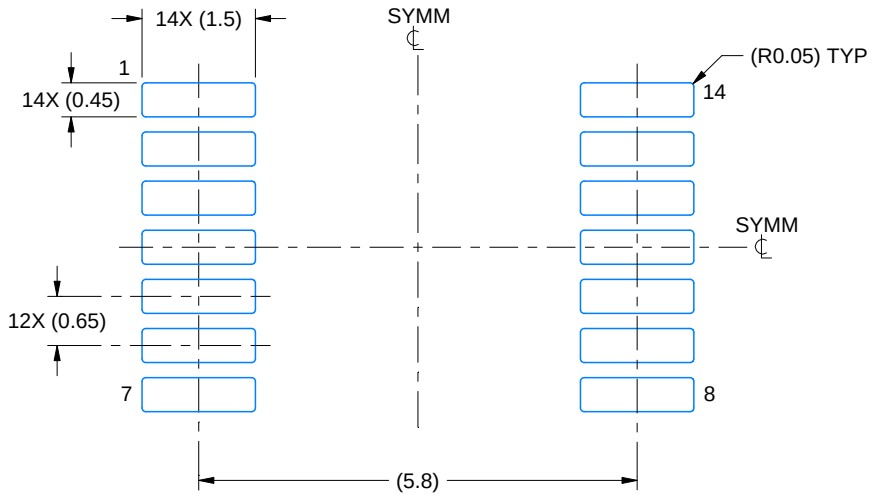
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

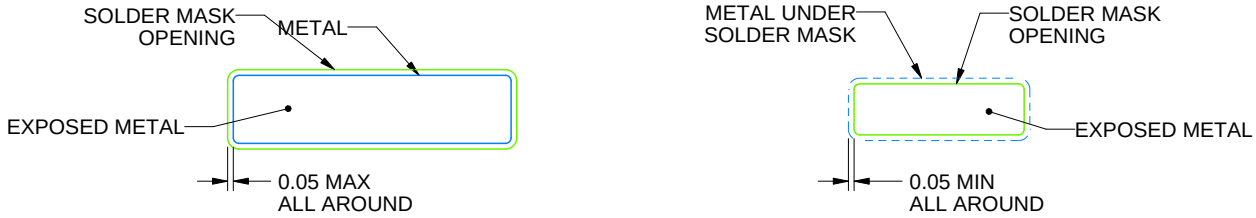


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

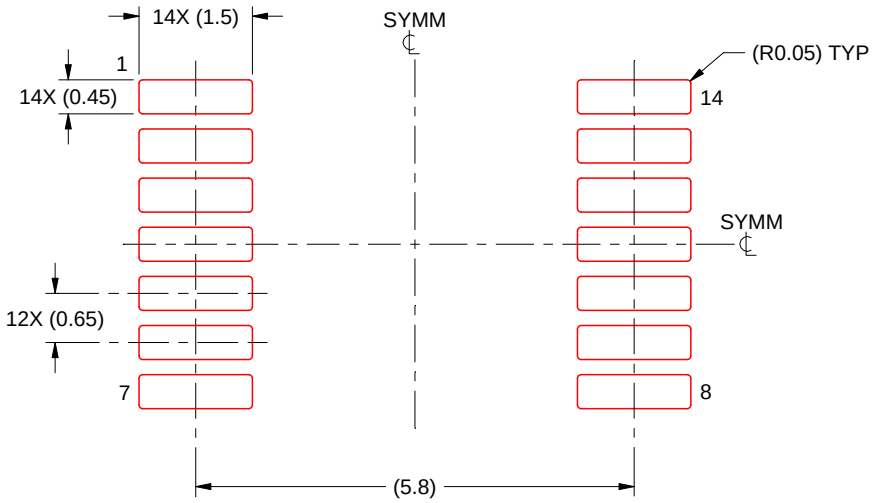


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

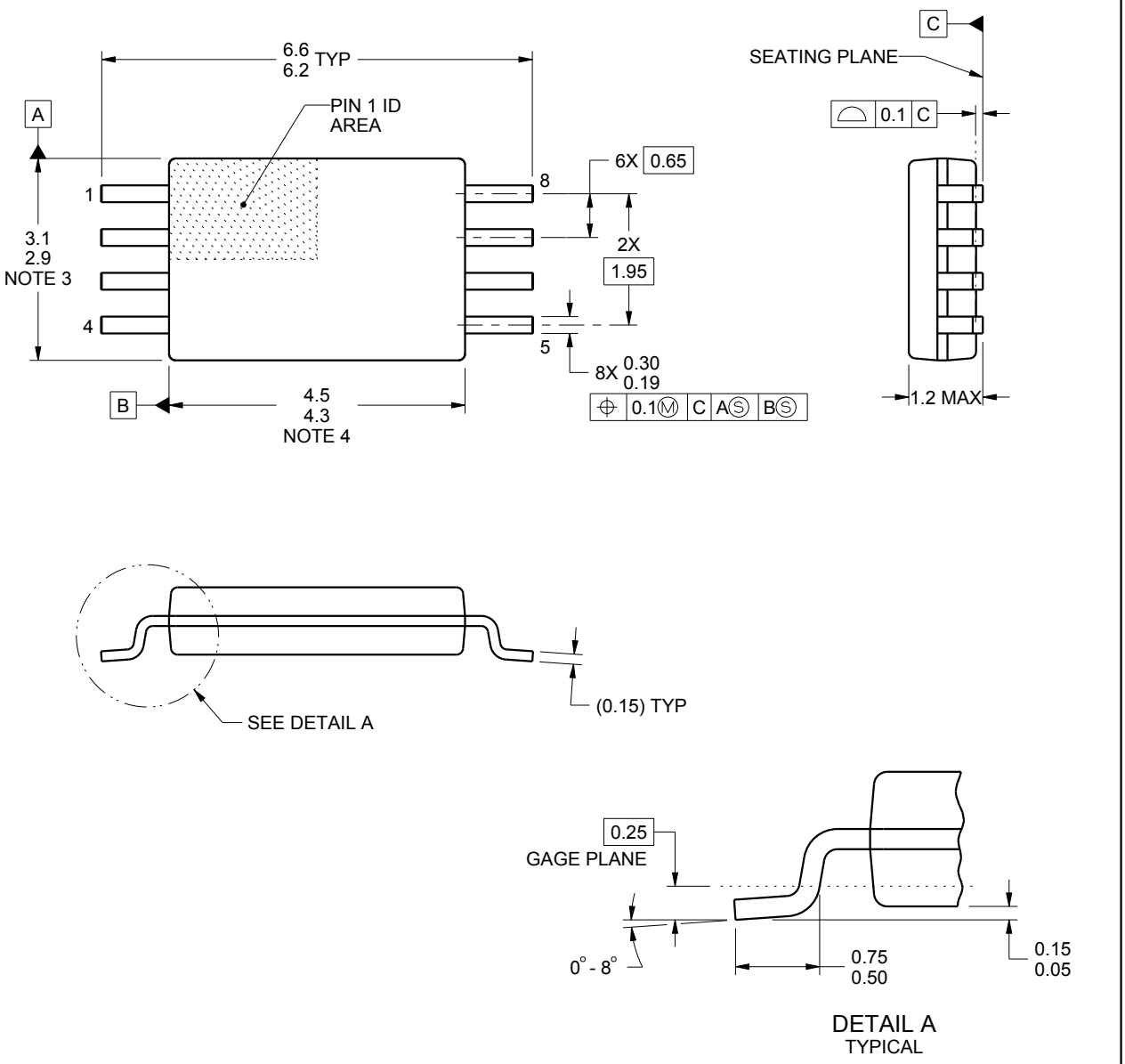
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

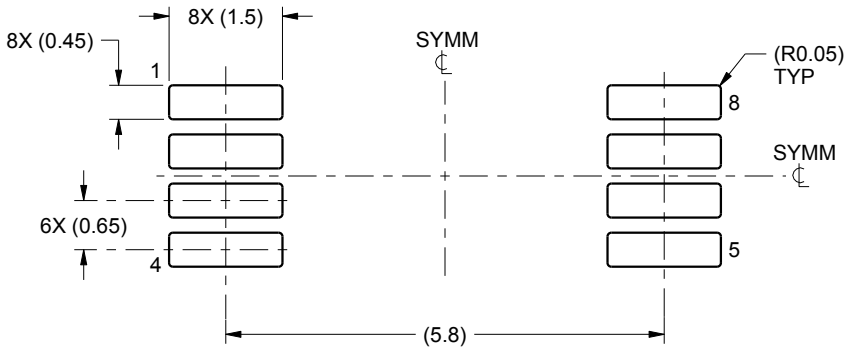
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

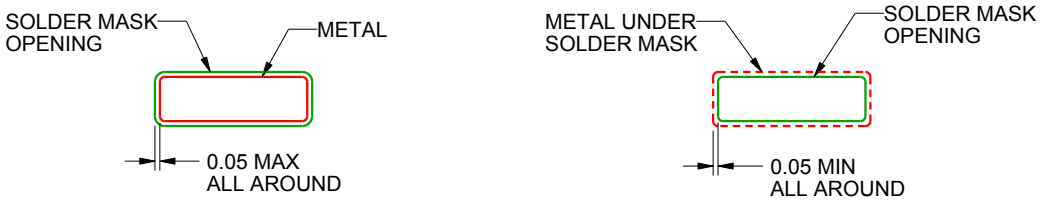


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

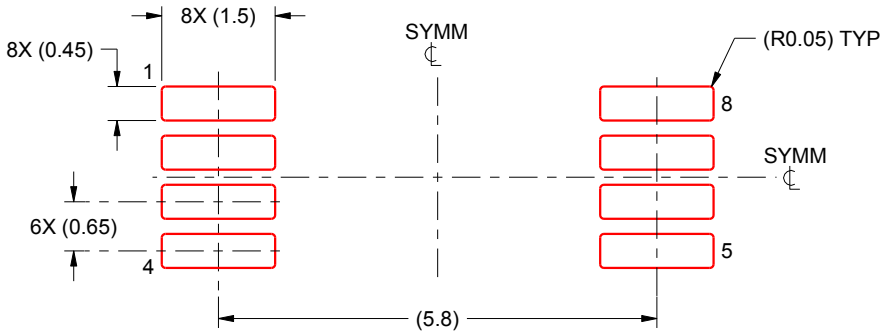


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月